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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3522US(97-1080)
First Inventor or Application Identifier	Mark McQueen
Title	ESD/EOS PROTECTION STRUCTURE FOR INTEGRATED CIRCUIT DEVICES AND METHODS OF FABRICATING THE SAME
Express Mail Label No.	EM548956862US

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages 26
(preferred arrangement set forth below)
-Descriptive title of the invention
-Cross References to related Applications
-Statement Regarding Fed Sponsored R&D
-Reference to Microfiche Appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings (*if filed*)
-Detailed Description
-Claim(s)
-Abstract of the Disclosure

3. ☒ Drawing(s) (*35 USC 113*) Total Sheets 40

4. Oath or Declaration Total Pages
a. ☐ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(For continuation/divisional with Box 17 completed)
(Note Box 5 below)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference (*useable if Box 4b is checked*)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
(*if applicable, all necessary*)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37CFR 3.73(b) Statement ☐ Power of Attorney
(*when there is an assignee*)
10. ☐ English Translation Document (*if applicable*)
11. ☐ Information Disclosure ☐ Copies of IDS
Statement (IDS/PTO-1449) Citations
12. ☐ Preliminary Amendment
13. ☐ Return Receipt Postcard (MPEP 503)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(*If foreign priority is claimed*)
16. ☐ Other: . . . . . .
. . . . . .
*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior Application No. _/
Prior application information: Examiner _____ Group/Art Unit: __

18. CORRESPONDENCE ADDRESS

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PTO/SB/17 (1/98)
Approved for use through 9/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT ($) 1,294.00

Complete if Known	
Application Number	To be assigned
Filing Date	September 3, 1998
First Named Inventor	Mark McQueen
Examiner Name	To be assigned
Group / Art Unit	To be assigned
Attorney Docket No.	3522US (97-1080)

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 20-1469
Deposit Account Name: Trask, Britt & Rossa

[ ] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
[ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. [X] **Payment Enclosed:**
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	790
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 790.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims 28	-20** = 8	x	22	= 176
Independent Claims 7	- 3** = 4	x	82	= 328
Multiple Dependent				=

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 504.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	Robert G. Winkle			Reg. Number	37,474
Signature		Date	9/3/98	Deposit Account User ID	

PATENT
Attorney Docket 3522US(97-1080)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EM548956862US

Date of Deposit with USPS: September 3, 1998

Person Making Deposit: Jared Turner

APPLICATION FOR LETTERS PATENT

for

ESD/EOS PROTECTION STRUCTURE FOR INTEGRATED CIRCUIT DEVICES AND METHODS OF FABRICATING THE SAME

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ESD/EOS PROTECTION STRUCTURE FOR INTEGRATED CIRCUIT DEVICES AND METHODS OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to electrostatic discharge and electrical overstress protection devices and methods of fabricating same. More particularly, the present invention relates to protection devices having charge dissipating structures within the electrostatic discharge and electrical overstress protection devices.

State of the Art: Electrostatic discharge (hereinafter "ESD") and electrical overstress (hereinafter "EOS") are two common phenomenon that occur during human or mechanical handling of semiconductor integrated circuitry (hereinafter "IC") devices. The input pins to an IC device are highly sensitive to damage from the voltage spike of an ESD, which can reach potentials in excess of hundreds of volts. If a charge of this magnitude is brought into contact with a pin of an IC device, a large flow of current may surge through the IC device. Although this current surge may be of limited energy and duration, it can cause a breakdown of insulating barriers within the IC device (usually gate oxide insulating barriers of an MOS (metal-oxide-semiconductor) IC device). This breakdown of the insulating barriers within an IC can result in permanent damage to the IC device and, once damaged, it is impossible to repair the IC device.

All pins of a MOS IC must be provided with protective circuits to prevent such ESD voltages from damaging the insulating barriers (e.g., gate oxide) therein. The most common ESD protection schemes presently used in MOS ICs rely on the parasitic bipolar transistors associated with an nMOS (n-channel or negative channel metal-oxide-semiconductor) device. These protective circuits are normally placed between the input and output pads (i.e., pin locations) on a semiconductor chip (which contains the IC device) and the transistor gates to which the input and output pads are electrically connected. With such protective circuits under stress conditions, the

dominant current conduction path between the protected pin and ground involves the parasitic bipolar transistor of that nMOS device. This parasitic bipolar transistor operates in the snapback region under pin positive with respect to ground stress events. The dominant failure mechanism found in the nMOS protection device operating in snapback conditions is the onset of second breakdown. Second breakdown is a phenomena that induces thermal runaway in the IC device wherever the reduction of the ESD current is offset by the thermal generation of carriers. Second breakdown is initiated in an IC device under stress, known as electrical overstress or EOS, as a result of self-heating. The peak nMOS device temperature at which second breakdown is initiated is known to increase with the stress current level. The time required for the structure to heat-up to this critical temperature is dependent on the device layout and stress power distributed across the device.

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated IC devices are ongoing goals of the computer industry. The advantage of increased miniaturization of components include: reduced-bulk electronic equipment, improved reliability by reducing the number of solder or plug connections, lower assembly and packaging costs, and improved circuit performance. In pursuit of increased miniaturization, IC devices have been continually redesigned to achieve ever higher degrees of integration, which has reduced the size of the IC device. However, as the dimensions of the IC devices are reduced, the geometry of the circuit elements have also decreased. In MOS IC devices, the gate oxide thickness has decreased to below 10 nanometers (nm), and breakdown voltages are often less than 10 volts. With decreasing geometries of the circuit elements, the failure susceptibility of IC device to ESD and EOS increases, and, consequently, providing adequate levels of ESD/EOS protection, has become increasingly more difficult.

An exemplary method of fabricating an ESD/EOS protection structure (i.e., bipolar transistor) is illustrated in FIGs. 29-38. FIG. 29 illustrates a first intermediate

structure 200 in the production of a bipolar transistor. This first intermediate structure 200 comprises a semiconductor substrate 202, such as a lightly doped P-type silicon substrate, which has been oxidized to form thick field oxide areas 204 and exposed to an implantation processes to form an n-type source region 206 and an n-type drain region 208. A transistor gate member 212 is formed on the surface of the semiconductor substrate 202 residing on a substrate active area 214 spanned between the source region 206 and the drain region 208. The transistor gate member 212 comprises a lower buffer layer 216 separating a gate conducting layer 218 of the transistor gate member 212 from the semiconductor substrate 202. Transistor insulating spacer members 222 are formed on either side of the transistor gate member 212. A cap insulator 224 is formed on the top of the transistor gate member 212. An insulative barrier layer 226 is disposed over the semiconductor substrate 202, the thick field oxide areas 204, the source region 206, the drain region 208, and the transistor gate member 212.

As shown in FIG. 30, an etch mask 232 is patterned on the surface of the insulative barrier layer 226, such that openings 234 in the first etch mask 232 are located substantially over the source region 206 and the drain region 208. The insulative barrier layer 226 is then etched through openings 234 to form vias 236 which expose a least a portion of the source region 206 and the drain region 208, as shown in FIG. 31. The etch mask 232 is then removed, as shown in FIG. 32. A first conductive material 238 is deposited over the insulative barrier layer 226 to fill the vias 236, as shown in FIG. 33. The first conductive material 238 is planarized, as shown in FIG. 34, to electrically separate the first conductive material 238 within each via 236 (see FIG. 33), thereby forming contacts 242. The planarization is usually performed using a mechanical abrasion process, such as a CMP.

A deposition mask 244 is patterned on the insulative barrier layer 226, having openings 246 over the contacts 242, as shown in FIG. 35. A second conductive material 248 is deposited over the deposition mask 244 to fill the deposition mask

openings 246, as shown in FIG. 36. The second conductive material 248 is planarized, as shown in FIG. 37, to electrically separate the second conductive material 248 within each deposition mask opening 246 (see FIG. 35). The planarization is usually performed using a mechanical abrasion, such as a CMP process. The deposition mask 244 is then removed to leave the second conductive material forming a source contact metallization 252 and a drain contact metallization 254, as shown in FIG. 38.

Although methods as described above are used in the industry, it is becoming more difficult to control the proper alignment of the etch mask 232 for the formation of the contacts 242 as tolerances become more and more stringent. For example, as shown in FIGs. 39 and 40, misalignment of the etch mask 232 can occur. Thus, as shown in FIG. 40, when the insulative barrier layer 226 is etched through the misaligned etch mask 232 to form a first via 256 and a second via 258, the etch forming the first via 256 can destroy a portion of the transistor insulating spacer member 222 and/or the cap insulator 224 to expose the gate conducting layer 218 of the transistor gate member 212. Thus, when a conductive material (not shown) is deposited in the first via 256, the gate conducting layer 218 will short, rendering the bipolar transistor ineffectual. Furthermore, the misaligned etch mask 232 can also result in the second via 258 exposing a portion of the field oxide area 204. However, since the etch to form the second 258 is generally an oxide insulator-type etch, the etch may also etch through the isolation oxide 204 to found a third via 262 thereby exposing a portion of the semiconductor substrate 202. Thus, when a conductive material (not shown) is deposited in the second via 258, the conductive material may short with the exposed portion of the semiconductor substrate 202.

Therefore, it would be desirable to design a bipolar transistor which can be fabricated with less sensitively to misalignment and which has a more efficient charge dissipating structures to handle electrostatic discharge and electrical overstress.

SUMMARY OF THE INVENTION

The present invention relates methods of forming an electrostatic discharge and electrical overstress protection devices for integrated circuits and devices so formed. The protection devices comprise at least one bipolar transistor which includes a shared electrical contacts within source regions and within drain regions for more efficient dissipation of an electrostatic discharge which, in turn, reduces the incidence of electrical overstress. The protection devices further include contact plugs and contact landing pads which renders the fabrication of such devices less sensitive to alignment constraint in the formation of contacts for the protection device.

An exemplary method of fabrication of the bipolar transistor of the present application comprises forming intermediate structure including a semiconductor substrate, such as a lightly doped P-type silicon substrate, which has been oxidized to form thick field oxide areas and exposed to n-type implantation processes to form a source region and a drain region. A transistor gate member is formed on the surface of the semiconductor substrate residing on a substrate active area spanned between the source region and the drain region. The transistor gate member comprises a lower buffer layer separating the gate conducting layer of the transistor gate member from the semiconductor substrate. Transistor insulating spacer members, preferably silicon dioxide, are formed on either side of the transistor gate member and a cap insulator is formed on the top of the transistor gate member.

A first barrier layer, preferably tetraethyl orthosilicate - TEOS, is disposed over the semiconductor substrate, the thick field oxide areas, the source region, the drain region, and the transistor gate member. A second barrier layer (preferably made of borophosphosilicate glass - BPSG, borosilicate glass - BSG, phosphosilicate glass - PSG, or the like) is deposited over the first barrier layer. It is, of course, understood that a single barrier layer could be employed. However, a typical barrier configuration is a layer of TEOS over the transistor gate member and the substrate followed by a BPSG layer over the TEOS layer. The TEOS layer is applied to prevent dopant

migration. The BPSG layer contains boron and phosphorus which can migrate into the source and drain regions formed on the substrate during inherent device fabrication heating steps. This migration of boron and phosphorus can change the dopant concentrations in the source and drain regions, which can adversely affect the performance of the transistor gate member.

The second barrier layer is then planarized down to the transistor gate member. The planarization is preferably performed using a mechanical abrasion, such as a chemical mechanical planarization (CMP) process. A first etch mask is patterned on the surface of the planarized second barrier layer, such that openings in the first etch mask are located substantially over the source region and the drain region. The first etch mask openings may be of any shape or configuration, including but not limited to circles, ovals, rectangles, or even long slots extending over several source regions or drain regions, respectively. The second barrier layer and first barrier layer are then etched to form first vias which expose at least a portion of the source region and the drain region, and the first etch mask is removed. The exposure of the transistor gate member and the etching of such a shallow second barrier layer and first barrier layer allows for easy alignment of the first etch mask which, of course, virtually eliminates the possibly of etching through the insulating material of the transistor gate member to expose and short the gate conducting layer within the transistor gate member. A first conductive material is deposited to fill the first vias. The first conductive material is then planarized to isolate the first conductive material within the first vias, thereby forming contact plugs.

Although any shape of openings in the first etch mask can be used, such as individual openings for each source and drain region, it is preferred that a plurality of the bipolar transistors are formed in parallel, such that long, slot-type openings in the first etch mask can be formed. The long slot-type opening, upon etching, forms long, slot vias which expose multiple source regions or multiple drain regions, respectively. Thus, when the first conductive material is deposited in the first vias, the first

conductive material will span multiple source or drain regions and, thereby, dissipate an ESD more efficiently.

A deposition mask is patterned on the second barrier layer, having openings over the contact plugs. The deposition mask openings may be of any shape or configuration, including but not limited to circles, ovals, rectangles, or even long slots extending over several source regions and drain regions, respectively. A second conductive material is deposited over the deposition mask to fill the deposition mask openings. The second conductive material is planarized to electrically separate the second conductive material within each deposition mask opening. The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The deposition mask is then removed to leave the second conductive material forming contact lands which are preferably wider than the contact plugs. Again, it is preferred that the contact lands extend over multiple source or drain regions to assist in the dissipation of an ESD.

A third barrier layer (preferably made of borophosphosilicate glass - BPSG, phosphosilicate glass - PSG, or the like) is deposited over the second barrier layer and the contact lands, and, optionally, planarized. A second etch mask is patterned on the third barrier layer, wherein the second etch mask includes openings substantially aligned over the contact lands. The third barrier layer is then etched down to the contact lands to form contact vias. As mentioned above, the contact lands are preferably larger than the contact plugs. The larger contact lands provide a bigger "target" for the etch through the third barrier layer to "hit" the contact lands in the formation of the contact vias. Thus, precise alignment becomes less critical.

The second etch mask is then removed and a third conductive material is deposited over the third barrier layer to fill the contact vias. The third conductive material is then planarized down to the third barrier layer, such as by a CMP method, to electrically isolate the conductive material within each contact via to form upper contacts. A second deposition mask is patterned on the third barrier layer, having

openings over the upper contacts. A fourth conductive material is deposited over the deposition mask to fill the deposition mask openings. The fourth conductive material is planarized to electrically separate the fourth conductive material within each deposition mask opening. The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The second deposition mask is then removed to leave the fourth conductive material forming source contact metallization and a drain contact metallization, thereby completing the formation of the bipolar transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is a side cross-sectional view of an intermediate structure in a method of forming an ESD/EOS protection structure according to the present invention;

FIG. 2 is a top plan view along line 2-2 of FIG. 1 illustrating a plurality of intermediate structures;

FIG. 3 is a side cross-sectional view of the intermediate structure after planarization of a barrier layer according to the present invention;

FIG. 4 is a side cross-sectional view of a etch mask patterning over the structure of FIG. 3 according to the present invention;

FIG. 5 is a side cross-sectional view of the structure of FIG. 4 after etching according to the present invention;

FIG. 6 is a side cross-sectional view of the structure of FIG. 5 after removal of the etch mask according to the present invention;

FIG. 7 is a top plan view of the structure of FIG. 6, wherein long, slot-type openings are used to form long, slot vias according to the present invention;

FIG. 8 is a top plan view of the structure of FIG. 6, wherein oval openings over each source and drain region respectively are used to form individual vias according to the present invention;

FIG. 9 is a side cross-sectional view of the structure of FIG. 6 after the deposition of a first conductive material to contact source and drain regions according to the present invention;

FIG. 10 is a side cross-sectional view of the structure of FIG. 9 after the planarization of the first conductive material according to the present invention;

FIG. 11 is a side cross-sectional view of the structure of FIG. 10 after the patterning of a deposition mask according to the present invention;

FIG. 12 is a side cross-sectional view of the structure of FIG. 11 after the deposition on a second conductive material according to the present invention;

FIG. 13 is a side cross-sectional view of the structure of FIG. 12 after the planarization of the second conductive material according to the present invention;

FIG. 14 is a side cross-sectional view of the structure of FIG. 13 after the removal of the deposition mask according to the present invention;

FIG. 15 is a top plan view of the structure of FIG. 14, wherein long, slot-type opening are used to form long contact lands form the second conductive material according to the present invention;

FIG. 16 is a top plan view of the structure of FIG. 14, wherein oval openings are used to form multiple, individual contact lands according to the present invention;

FIG. 17 is a side cross-sectional view of the structure of FIG. 14 after the deposition of a third barrier layer according to the present invention;

FIG. 18 is a side cross-sectional view of the structure of FIG. 17 after the patterning of a second etch mask according to the present invention;

FIG. 19 is a side cross-sectional view of the structure of FIG. 18 after the etching of the third barrier layer to form contact vias according to the present invention;

FIG. 20 is a side cross-sectional view of the structure of FIG. 19 after the removal of the second etch mask according to the present invention;

FIG. 21 is a side cross-sectional view of the structure of FIG. 20 after the deposition of a third conductive material to fill the contact vias according to the present invention;

FIG. 22 is a side cross-sectional view of the structure of FIG. 21 after the planarization of the third conductive material according to the present invention;

FIG. 23 is a side cross-sectional view of the structure of FIG. 22 after the patterning of a deposition mask according to the present invention;

FIG. 24 is a side cross-sectional view of the structure of FIG. 23 after the deposition of a fourth conductive material according to the present invention;

FIG. 25 is a side cross-sectional view of the structure of FIG. 24 after the planarization of the fourth conductive material according to the present invention;

FIG. 26 is a side cross-sectional view of the structure of FIG. 25 after the removal of the second deposition mask to form a source contact metallization and a drain contact metallization according to the present invention;

FIG. 27 is a top plane view of the source contact metallization and the drain contact metallization according to the present invention;

FIG. 28 is a schematic of the ESD/EOS protection structure between the drain input pad and integrated circuitry to be protected according to the present invention;

FIGs. 29-38 are side cross-sectional views of an exemplary method of forming a bipolar transistor; and

FIGs. 39-40 are side cross-sectional views of the exemplary method of FIGs. 29-38 for forming a bipolar transistor wherein an etch mask is misaligned during fabrication thereof.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGs. 1-28 illustrate various view of techniques according to the present invention for forming ESD/EOS protection structures. It should be understood that the figures presented in conjunction with this description are not meant to be actual cross-sectional views of any particular portion of an actual semiconductor device, but are merely idealized representations which are employed to more clearly and fully depict the process of the invention than would otherwise be possible. Elements common between the figures maintain the same numeric designation.

FIG. 1 illustrates a first intermediate structure 100 in the production of a bipolar transistor. This first intermediate structure 100 comprises a semiconductor substrate 102, such as a lightly doped P-type silicon substrate, which has been oxidized to form thick field oxide areas 104 and exposed to n-type implantation processes to form a source region 106 and a drain region 108. A transistor gate member 112 is formed on the surface of the semiconductor substrate 102 residing on a substrate active area 114 spanned between the source region 106 and the drain region 108. The transistor gate member 112 comprises a lower buffer layer 116, preferably silicon dioxide, separating a gate conducting layer 118 of the transistor gate member 112 from the semiconductor substrate 102. Transistor insulating spacer members 122, preferably silicon dioxide or silicon nitride, are formed on either side of the transistor gate member 112 and a cap insulator 124, also preferably silicon dioxide or silicon nitride, is formed on the top of the transistor gate member 112.

A first barrier layer 126, preferably tetraethyl orthosilicate - TEOS, is disposed over the semiconductor substrate 102, the thick field oxide areas 104, the source region 106, the drain region 108, and the transistor gate member 112. A second barrier layer 128 (preferably made of borophosphosilicate glass - BPSG, borosilicate glass - BSG, phosphosilicate glass - PSG, or the like) is deposited over the first barrier layer 126.

Generally, the plurality of structures, as shown in FIG. 1, are formed in multiple sets on the semiconductor substrate 102. FIG. 2 illustrates a top view of such a plurality of substrate active areas 114 surrounded by the thick field oxide area 104, wherein the substrate active areas 114 include the source regions 106, the drain regions 108, and the transistor gate member 112 spanning and intersecting the substrate active areas 114, prior to the deposition of the first barrier layer 126 and the second barrier layer 128.

As shown in FIG. 3, the second barrier layer 128 is then planarized down to the transistor gate member 112. The planarization is preferably performed using a mechanical abrasion, such as a chemical mechanical planarization (CMP) process. As shown in FIG. 4, a first etch mask 132, such as photoresist, is patterned on the surface of the planarized second barrier layer 128, such that openings 134 in the first etch mask 132 are located substantially over the source region 106 and the drain region 108. The etch mask openings 134 may be of any shape or configuration, including but not limited to circles, ovals, rectangles, or even long slots extending over several source regions 106 and drain region 108, respectively. The second barrier layer 128 and first barrier layer 126 are then etched to form first vias 136 to expose at least a portion of the source region 106 and the drain region 108, as shown in FIG. 5. The etch mask 132 is then removed to form a second intermediate structure 140, as shown in FIG. 6.

FIGs. 7 and 8 illustrate top plan views of the second intermediate structure 140 of FIG. 6, wherein different shape openings 134 of the etch mask 132 (see FIG. 5) were utilized. FIG. 7 is the resulting intermediate structure 140 wherein long, slot-type openings are utilized to form long, slot vias 142 which expose multiple source regions 106 and multiple drain regions 108, respectively. FIG. 8 is a resulting intermediate structure 140 wherein oval openings are utilized to form multiple, individual vias 144 which expose individual source regions 106 and individual drain

regions 108 (active areas 114, source regions 106, and drain regions 108 are shown in shadow for visual orientation).

As shown in FIG. 9, a first conductive material 146, such as n-type doped polysilicon, is deposited such that the first vias 136 are filled therewith. The first conductive material 146 is then planarized to isolate the first conductive material 146 within the first vias 136, thereby forming contact plugs 148, as shown in FIG. 10. Preferably, the first vias 136 are formed as long, slot vias 142, as shown in FIG. 7, as the first conductive material 146 in each slot via will span multiple source or drain regions and, thereby, dissipate an ESD more efficiently.

A deposition mask 152, such as TEOS, is patterned on the second barrier layer 128 having openings 154 over the contact plugs 148, as shown in FIG. 11. The deposition mask openings 152 may be of any shape or configuration, including but not limited to circles, ovals, rectangles, or even long slots extending over several source regions 106 and drain region 108, respectively. A second conductive material 156, such as n-doped polysilicon, is deposited over the deposition mask 152 to fill the deposition mask openings 154, as shown in FIG. 12. The second conductive material 156 is planarized, as shown in FIG. 13, to electrically separate the second conductive material 156 within each deposition mask opening 154 (see FIG. 11). The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The deposition mask 152 may be removed (optional) to leave the second conductive material forming contact lands 158 on a third intermediate structure 160, as shown in FIG. 14.

FIGs. 15 and 16 illustrate top plan views of the third intermediate structure 160 of FIG. 14, wherein different shape openings 154 of the deposition mask 152 (see FIG. 11) were utilized. FIG. 15 is the resulting intermediate structure 160 wherein long, slot-type openings are utilized to form long, contact lands 162 spanned over multiple source regions 106 (shown in shadow) and multiple drain regions 108 (shown in shadow), respectively (active areas 114, transistor gate members 112, and contact

plugs 148 (formed in the long, slot vias 142, as shown in FIG. 7) are also shown in shadow for visual orientation). FIG. 16 is the resulting intermediate structure 160 wherein oval openings are utilized to form multiple, individual contact lands 164 atop the contact plugs 148 formed in multiple, individual vias 144, as shown in FIG. 8 (contact plugs 148, source regions 106, drain regions 108, active areas 114, and gate members 112).

A third barrier layer 166 (preferably made of borophosphosilicate glass - BPSG, phosphosilicate glass - PSG, or the like) is deposited over the second barrier layer 128 and the contact lands 158, and, optionally, planarized, as shown in FIG. 17. A second etch mask 168, such as photoresist, is deposited on the third barrier layer 166, wherein the second etch mask 168 includes opening 172 substantially aligned over the contact lands 158, as shown in FIG. 18. The third barrier layer 166 is then etched down to the contact lands 158 to form contact vias 174, as shown in FIG. 19, and the second etch mask 168 is then removed, as shown in FIG. 20.

A third conductive material 176, such as titanium nitride or tungsten, is deposited over the third barrier layer 166 to fill the contact vias 174 (see FIG. 20), as shown in FIG. 21. The third conductive material 176 is then planarized down to the third barrier layer 166, such as by a CMP method, to electrically isolate the conductive material 176 within each contact via 174 to form upper contacts 178, as shown in FIG. 22.

A second deposition mask 180, such as TEOS, is patterned on the third barrier layer 166, having openings 182 over the upper contacts 178, as shown in FIG. 23. A fourth conductive material 184 is deposited over the deposition mask 180 to fill the deposition mask openings 182, as shown in FIG. 24. The fourth conductive material 184 is planarized, as shown in FIG. 25, to electrically separate the fourth conductive material 184 within each deposition mask opening 182 (see FIG. 23). The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The second deposition mask 180 is then removed to leave the fourth

conductive material forming source contact metallization 186 and a drain contact metallization 188 resulting in an ESD/EOS protection structure 190, as shown in FIG. 26.

FIG. 27 illustrates a top plane view of the source contact metallization 186 and the drain contact metallization 188. The source contact metallization 186 is in electrical communication with a source plate 194 and the drain contact metallization 188 is in contact with a drain input pad 192. The gates 112 are connected to a common electrical contact 196. The gates 112 and the upper contacts 178 are illustrated for visual orientation, but it is understood that they would not be visible with a top plan view. FIG. 28 illustrates a schematic of the ESD/EOS protection structure between the drain input pad 192 and integrated circuitry 198 to be protected.

It is, of course, understood that the present invention can be used to form any contact for a semiconductor device, wherein a contact plug (such as contact plug 148) is capped with a contact land (such as contact land 158) in order to make the formation of the contact less sensitive to etch misalignments.

* * * * *

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A contact for a semiconductor device, comprising:

a contact plug extending through a first barrier layer, wherein said contact plug is in electrical communication with an active region on a semiconductor substrate;

a contact land disposed atop said contact plug, wherein said contact land has a larger cross-sectional area than said contact plug;

an upper contact extending through a second barrier layer, which is disposed over said first barrier layer, to form an electrical contact with contact land.

2. A method of forming a contact for a semiconductor device, comprising:

providing a semiconductor substrate having at least one active region;

depositing a first barrier layer over said substrate;

forming a first opening through said first barrier layer to expose a portion of said active region;

filling said first opening with a first conductive material to form a contact plug;

forming a conductive contact land over said contact plug;

depositing a second barrier layer over said first barrier layer and said conductive contact land;

forming a second opening through said second barrier layer to expose a portion of said conductive contact land; and

filling said second opening with a second conductive material to form said contact.

3. A bipolar transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further

including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through a first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through a first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land has a larger cross-sectional area than said at least one drain contact plug;

at least one source contact land disposed atop said at least one source contact plug, wherein said at least one source contact land has a larger cross-sectional area than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, wherein said at least one upper source contact is in electrical communication with said at least one source contact land; and

at least one upper drain contact extending through said second barrier layer, wherein said at least one upper drain contact is in electrical communication with said at least one drain contact land.

4. The bipolar transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. The bipolar transistor of claim 3, wherein said source contact plug extends between at least two source regions.

6. The bipolar transistor of claim 3, wherein said drain contact plug extends between at least two drain regions.

7. The bipolar transistor of claim 3, wherein said source contact land extends between at least two source contact plugs.

8. The bipolar transistor of claim 3, wherein said drain contact land extends between at least two drain contact plugs.

9. The bipolar transistor of claim 3, wherein said upper source contact extends between at least two source contact lands.

10. The bipolar transistor of claim 3, wherein said upper drain contact extends between at least two drain contact lands.

11. A method of producing a bipolar transistor for the dissipation of electrostatic discharges, comprising:

providing an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said drain region and said source region on said substrate active area;

depositing a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

planarizing said first barrier layer to expose said at least one gate member;

patterning a first etch mask on said first barrier layer, wherein said first resist layer includes openings substantially over said at least one drain region and over said at least one source region;

etching said first barrier layer to expose said at least one drain region and said at least one source region in said substrate forming at least one drain via and at least one source via, respectively;

removing said first etch mask;

depositing a layer of first conductive material over said first etched barrier layer to fill said at least one drain via and said at least one source via;

planarizing said first conductive material forming at least one drain contact plug and at least one source contact plug in said at least one drain via and said at least one source via, respectively;

patterning a first deposition material on said first buffer layer and said at least one transistor gate member, wherein said first deposition material includes openings over said at least one drain contact plug and said at least one source contact plug;

depositing a layer of second conductive material over said first deposition material to fill said openings over said at least one drain contact plug and said at least one source contact plug;

planarizing said second conductive material to said first deposition material to form at least one drain contact land and at least one source contact land;

removing said first deposition material;

depositing a second barrier layer over said first barrier layer and said at least one drain contact land and at least one source contact land;

patterning a second etch mask on said second barrier layer, wherein said second resist layer includes openings substantially over said at least one drain contact land and over said at least one source contact land;

etching said second barrier layer to expose said at least one drain contact land and said at least one source contact land forming at least one drain contact via and at least one source drain via, respectively;

removing said second etch mask;

depositing a layer of third conductive material over said etched second barrier layer to fill said at least one drain contact via and said at least one source contact via; and

planarizing said third conductive material forming at least one upper drain contact and at least one upper source contact in said at least one drain contact via and said at least one source contact via, respectively.

12. The method of claim 11, further comprising:

patterning a second deposition material on said second buffer layer, said at least one upper drain contact, and said at least one upper source contact, wherein said first deposition material includes openings over said at least one upper drain contact and said at least one upper source contact;

depositing a layer of fourth conductive material over said second deposition material to fill said openings over said upper drain contact and said upper source contact;

planarizing said fourth conductive material to said second deposition material to form a drain contact metallization and a source contact metallization; and

removing said second deposition material.

13. The method of claim 11, wherein said source contact plug extends between at least two source regions.

14. The method of claim 11, wherein said drain contact plug extends between at least two drain regions.

15. The method of claim 11, wherein said source contact land extends between at least two source contact plugs.

16. The method of claim 11, wherein said drain contact land extends between at least two drain contact plugs.

17. The method of claim 11, wherein said upper source contact extends between at least two source contact lands.

18. The method of claim 11, wherein said upper drain contact extends between at least two drain contact lands.

19. A semiconductor device including at least one contact, comprising:
a contact plug extending through a first barrier layer, wherein said contact plug is in electrical communication with an active region on a semiconductor substrate;
a contact land disposed atop said contact plug, wherein said contact land has a larger cross-sectional area than said contact plug;
an upper contact extending through a second barrier layer, which is disposed over said first barrier layer, to form an electrical contact with contact land.

20. A method of forming a semiconductor device having at least one contact, comprising:
providing a semiconductor substrate having at least one active region;
depositing a first barrier layer over said substrate;
forming a first opening through said first barrier layer to expose a portion of said active region;
filling said first opening with a first conductive material to form a contact plug;
forming a conductive contact land over said contact plug;

depositing a second barrier layer over said first barrier layer and said conductive contact land;

forming a second opening through said second barrier layer to expose a portion of said conductive contact land; and

filling said second opening with a second conductive material to form said contact.

21. A semiconductor device including at least one bipolar transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through a first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through a first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least source region on said semiconductor substrate;

at least one drain contact land disposed atop said at least one drain contact plug, wherein said at least one drain contact land has a larger cross-sectional area than said at least one drain contact plug;

at least one source contact land disposed atop said at least one source contact plug, wherein said at least one source contact land has a larger cross-sectional area than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, wherein said at least one upper source contact is in electrical communication with said at least one source contact land; and

at least one upper drain contact extending through said second barrier layer, wherein said at least one upper drain contact is in electrical communication with said at least one drain contact land.

22. The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

23. The semiconductor device of claim 21, wherein said source contact plug extends between at least two source regions.

24. The semiconductor device of claim 21, wherein said drain contact plug extends between at least two drain regions.

25. The semiconductor device of claim 21, wherein said source contact land extends between at least two source contact plugs.

26. The semiconductor device of claim 21, wherein said drain contact land extends between at least two drain contact plugs.

27. The semiconductor device of claim 21, wherein said upper source contact extends between at least two source contact lands.

28. The bipolar transistor of claim 21, wherein said upper drain contact extends between at least two drain contact lands.

ABSTRACT

Apparatus and methods forming electrostatic discharge and electrical overstress protection devices for integrated circuits wherein such devices include shared electrical contact between source regions and between drain regions for more efficient dissipation of an electrostatic discharge. The devices further include contact plugs and contact lands which renders the fabrication of the devices less sensitive to alignment constraint in the formation of contacts for the device.

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FIG. 1

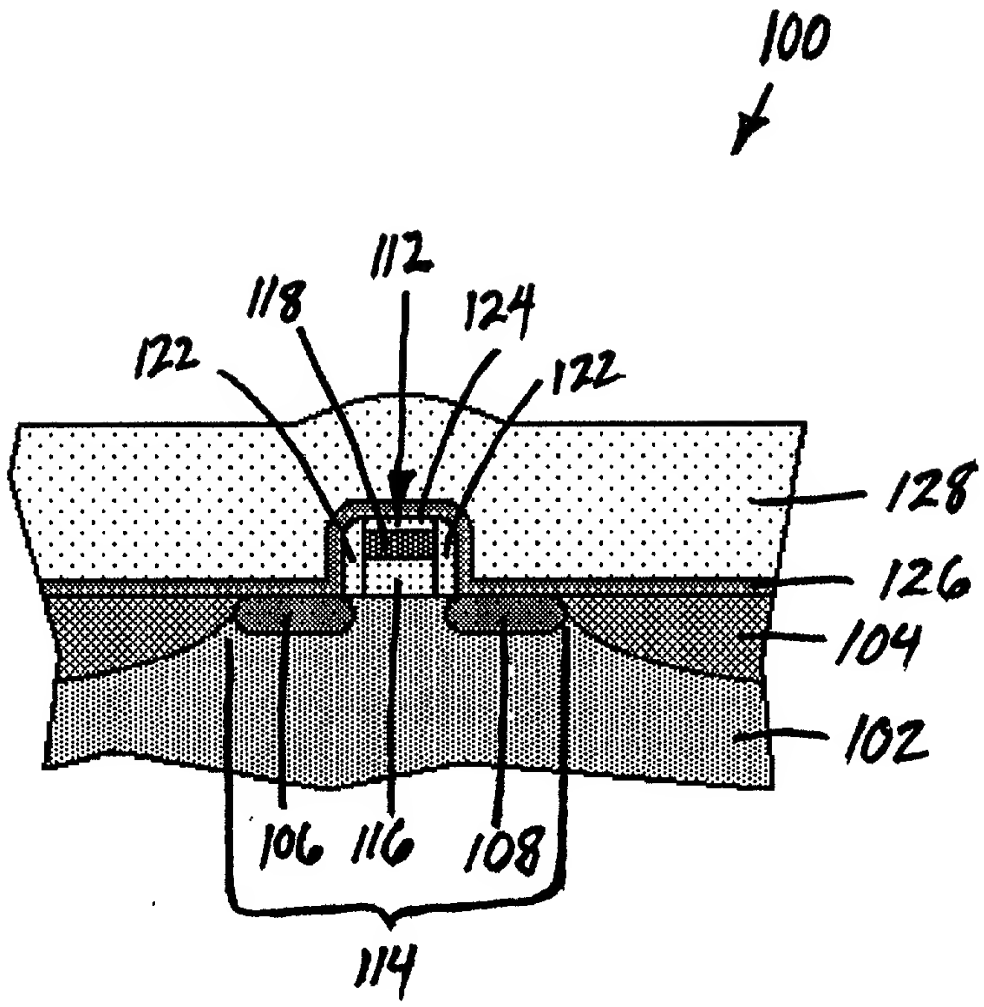

FIG. 2

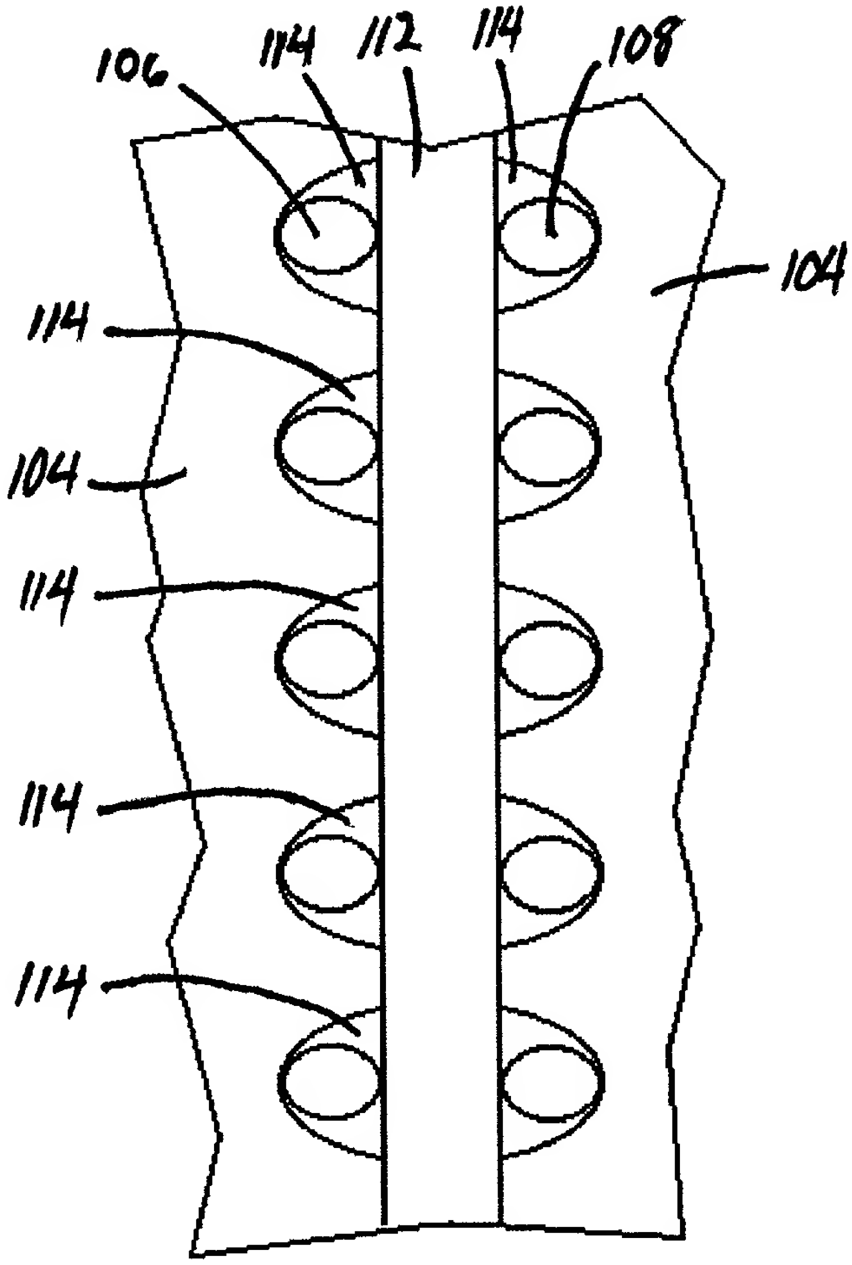

FIG. 3

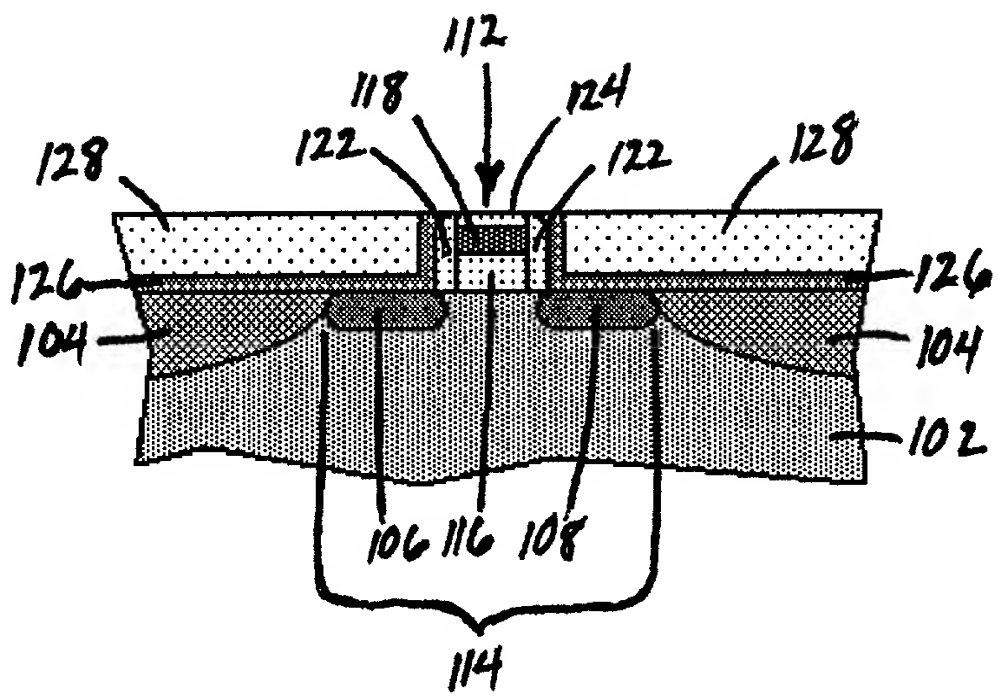

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FIG. 4

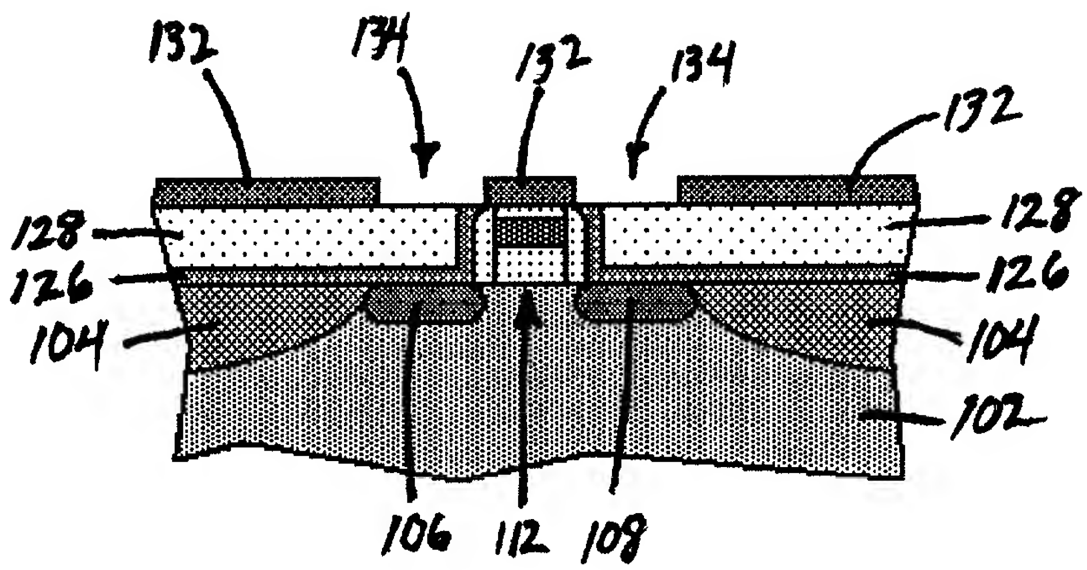

FIG. 5

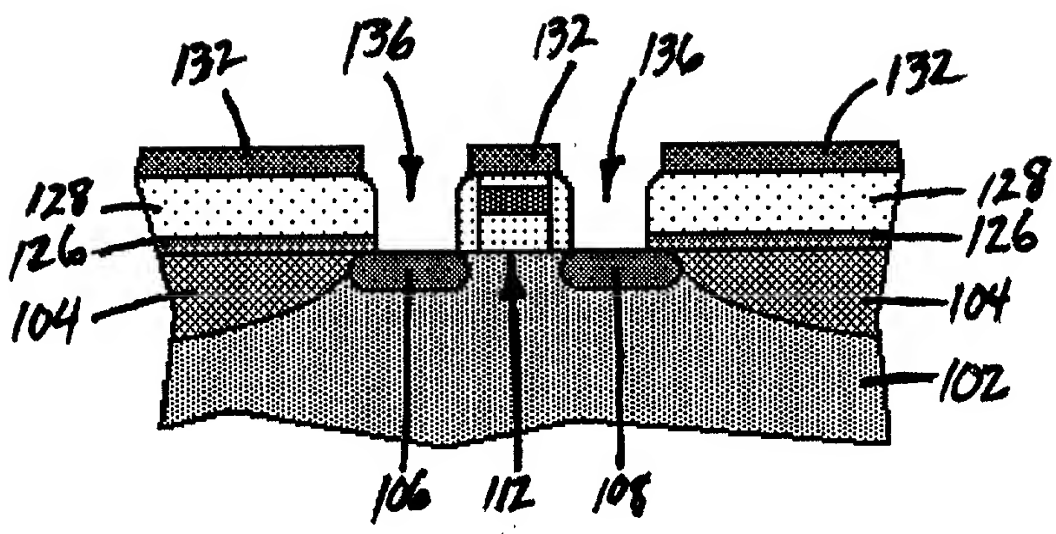

FIG. 6

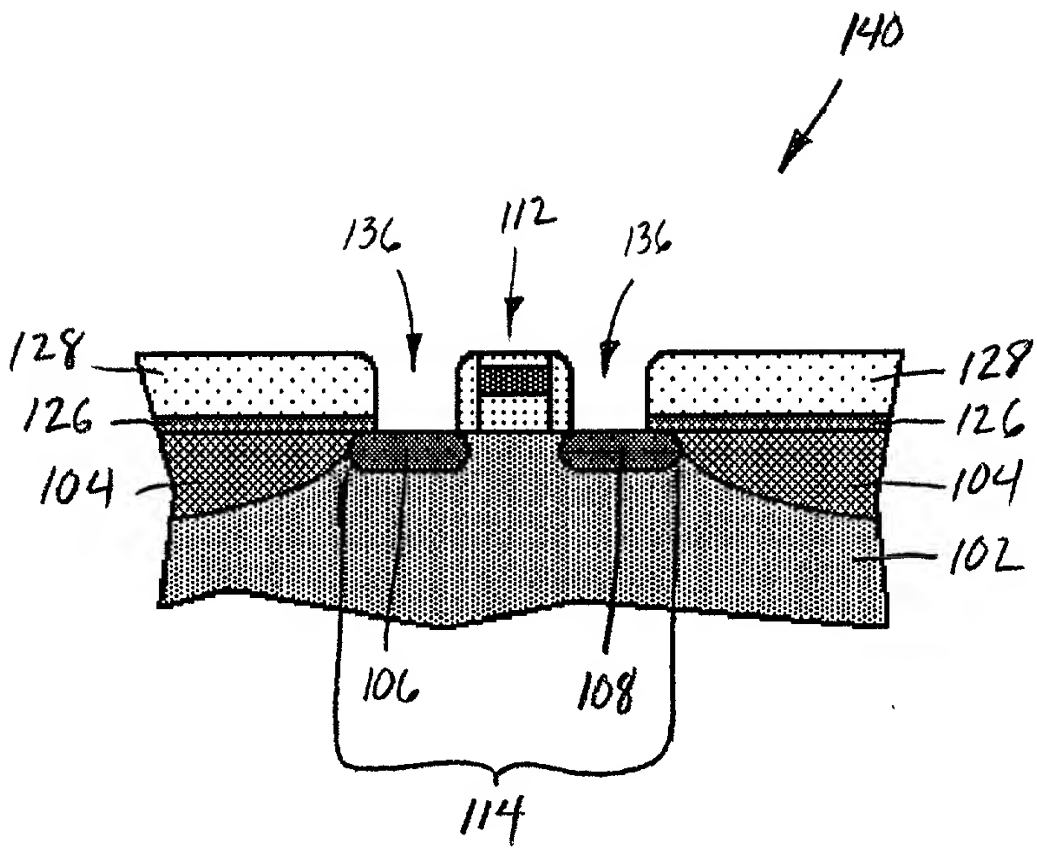

FIG. 7

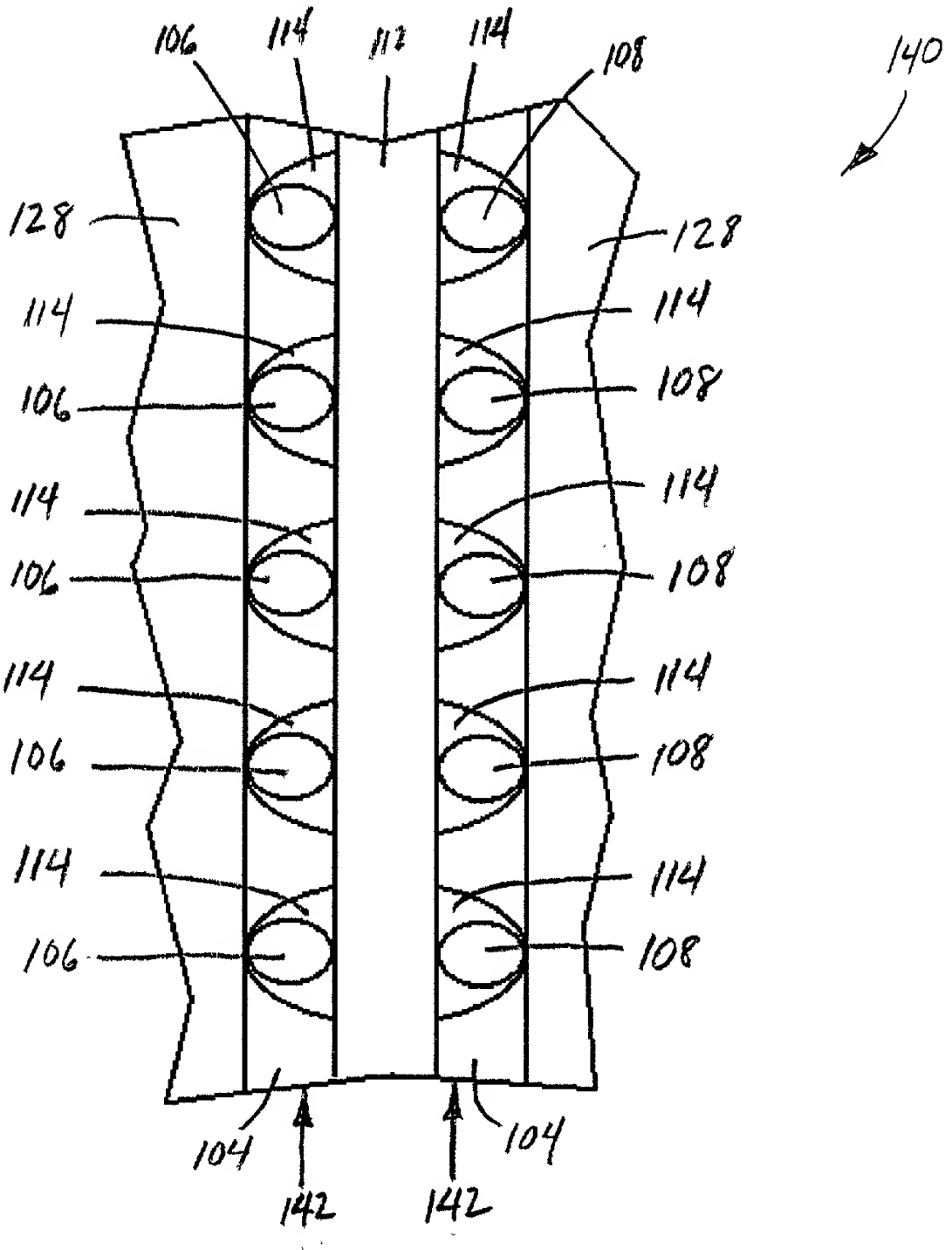

FIG. 8

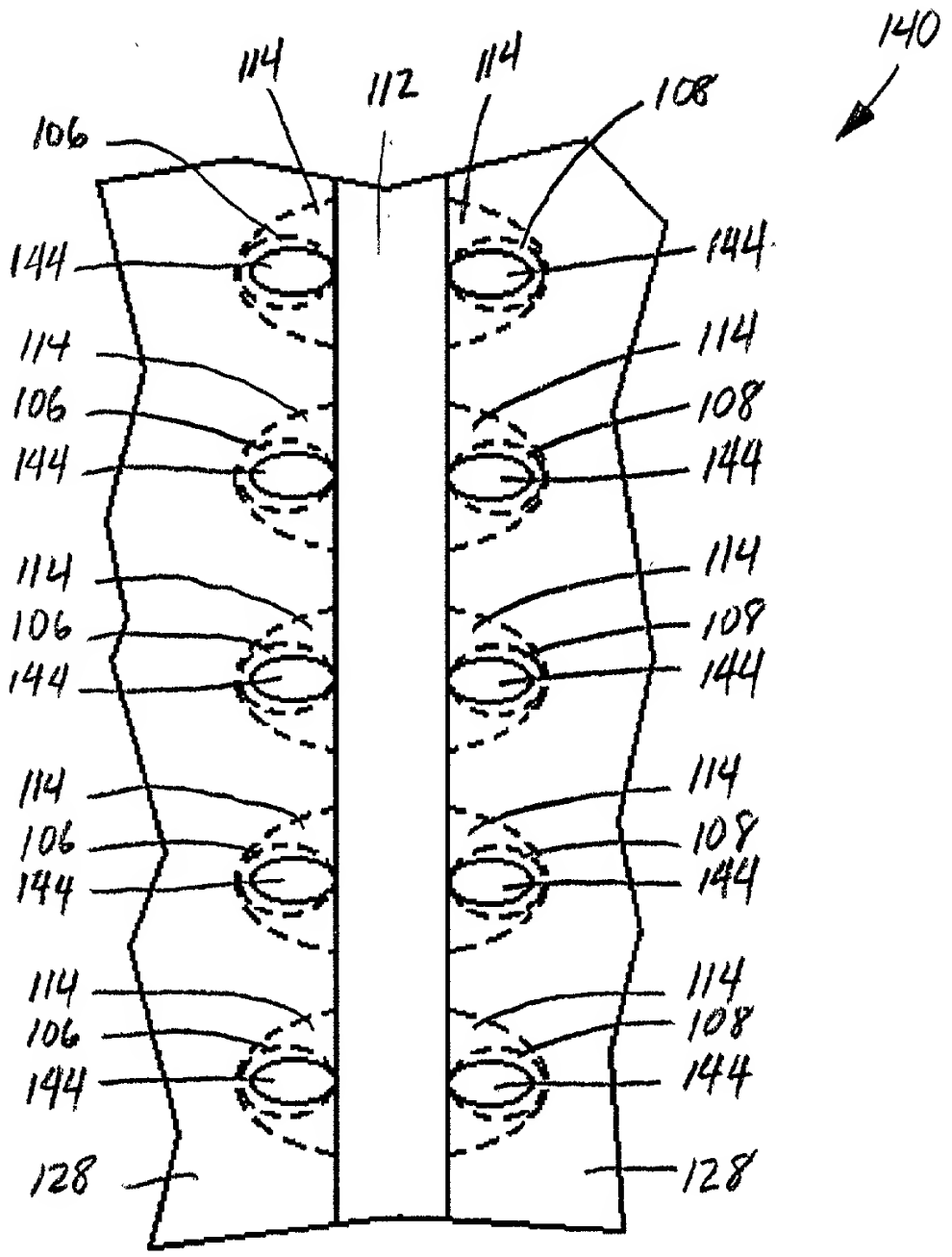
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FIG. 9

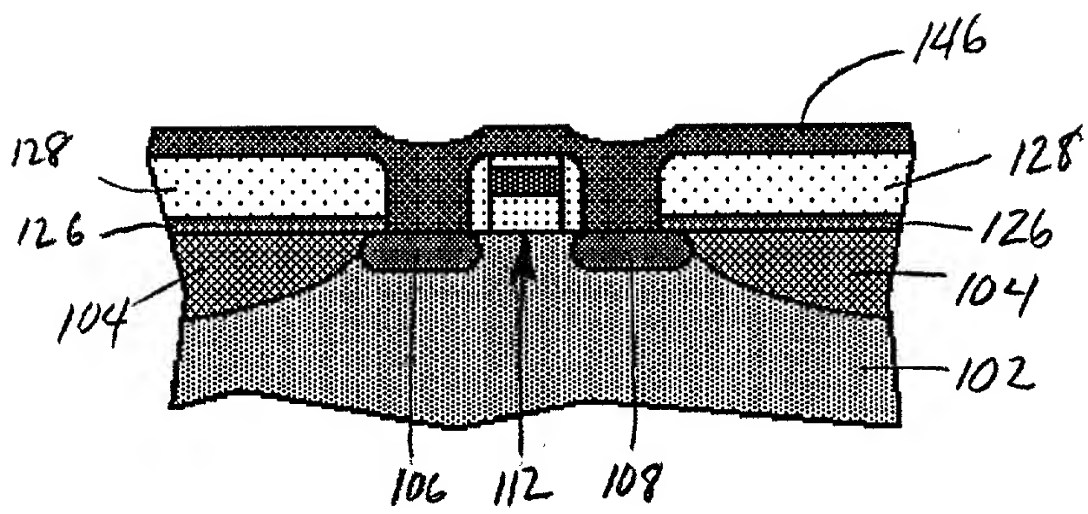

FIG. 10

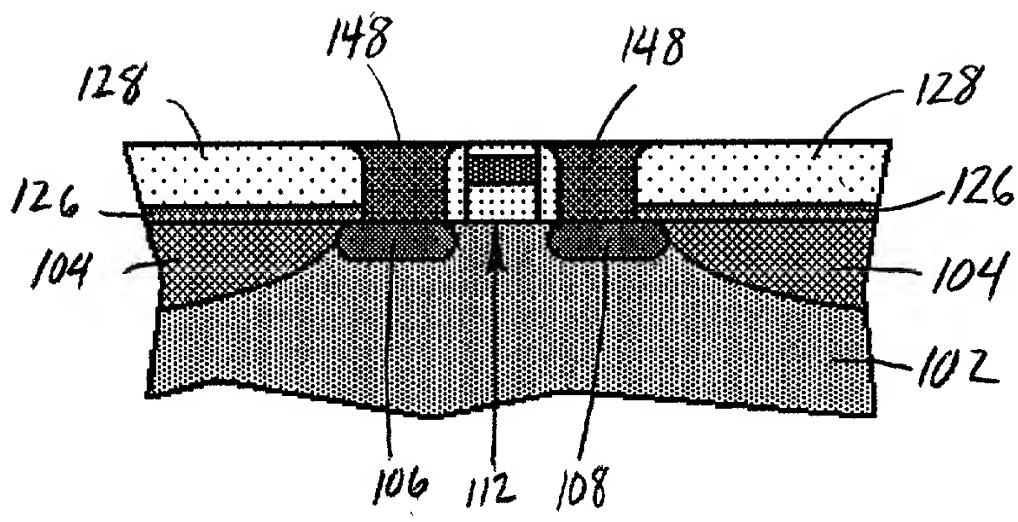

FIG. 11

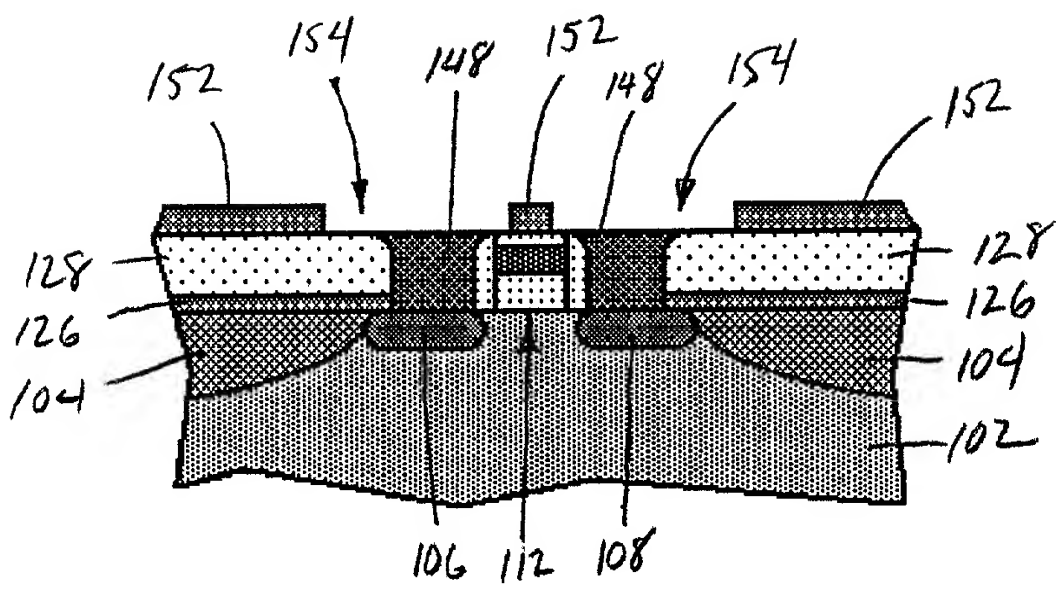

FIG. 12

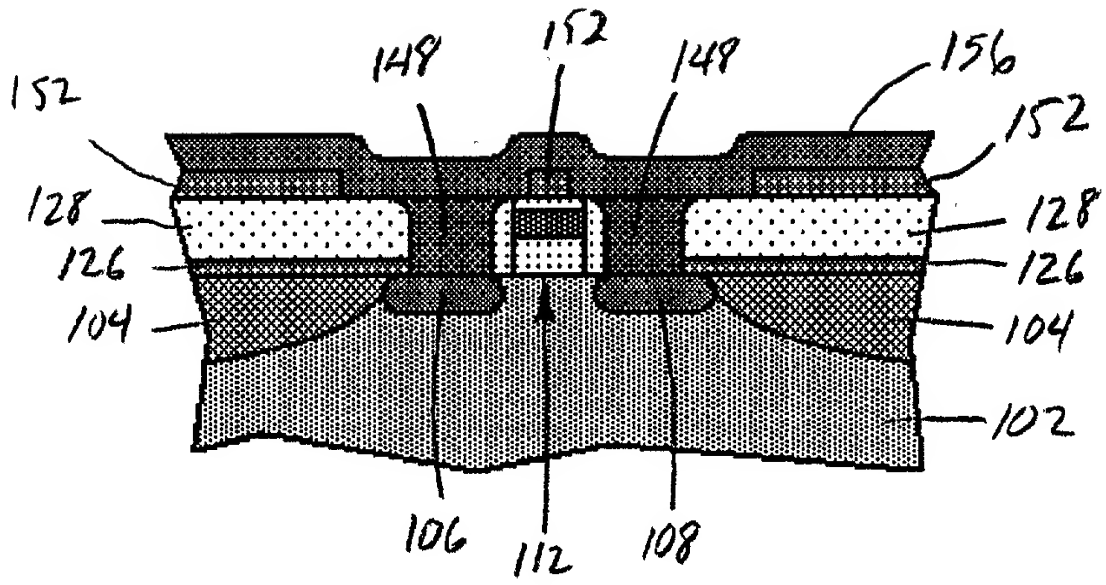

FIG. 13

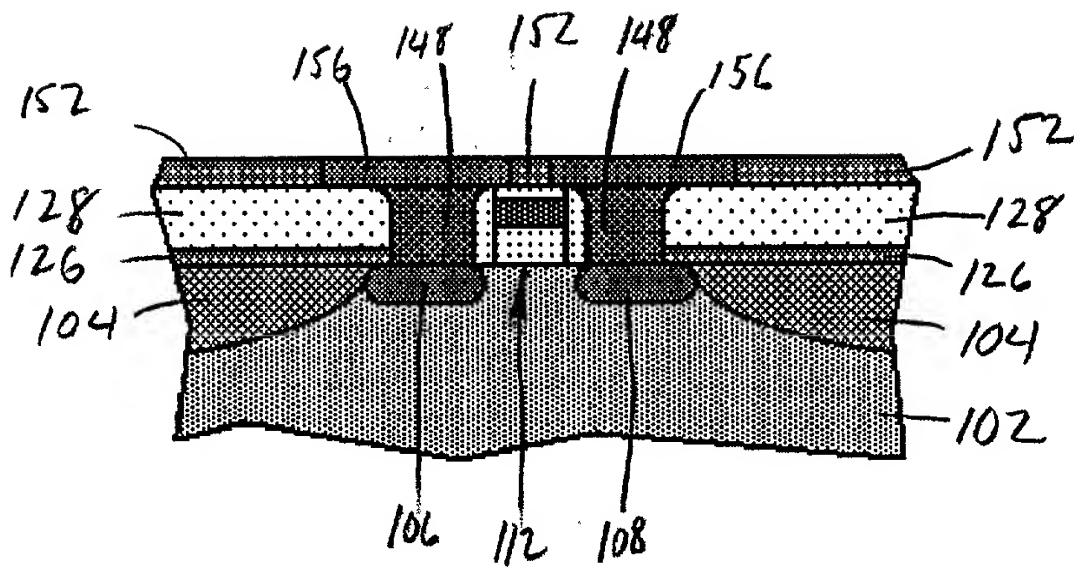

FIG. 14

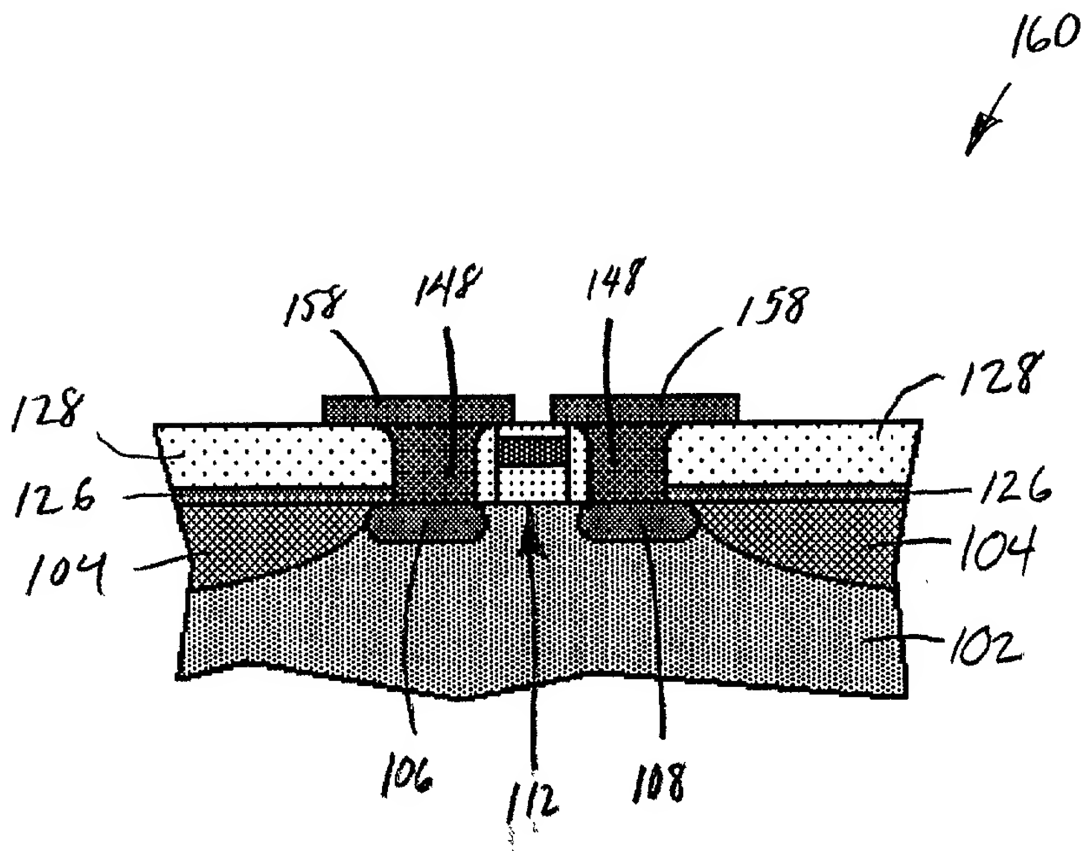

FIG. 15

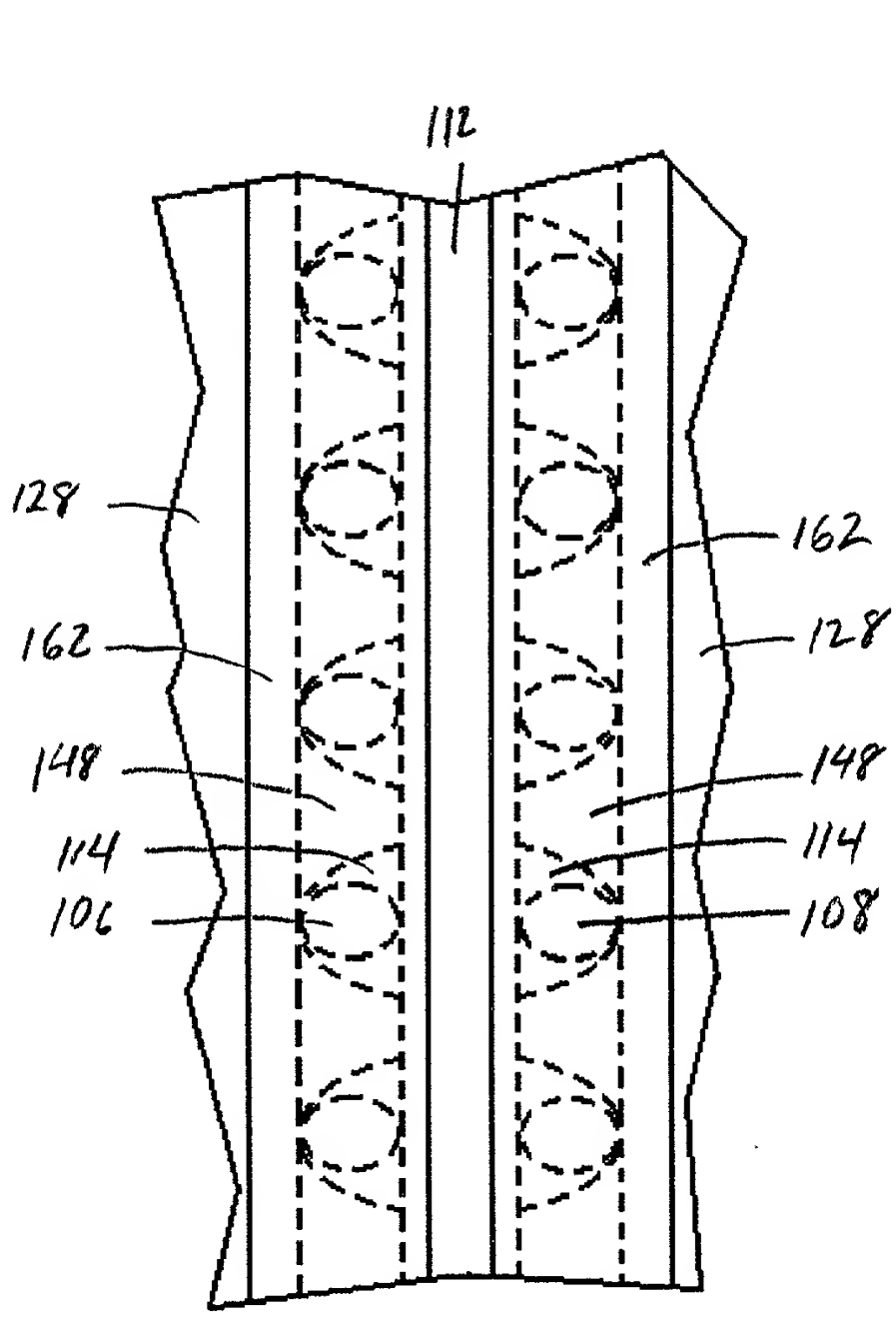

FIG. 16

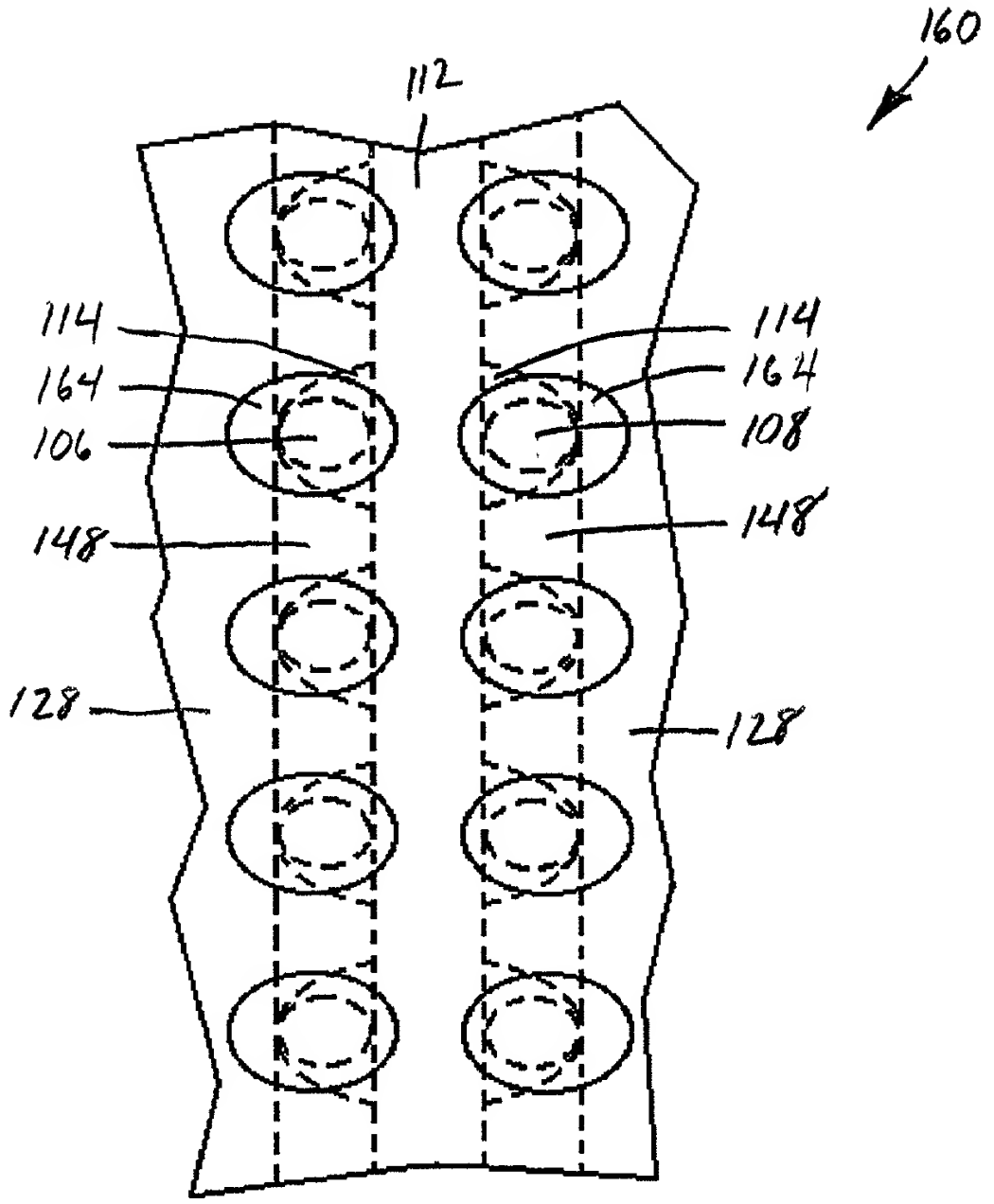

FIG. 17

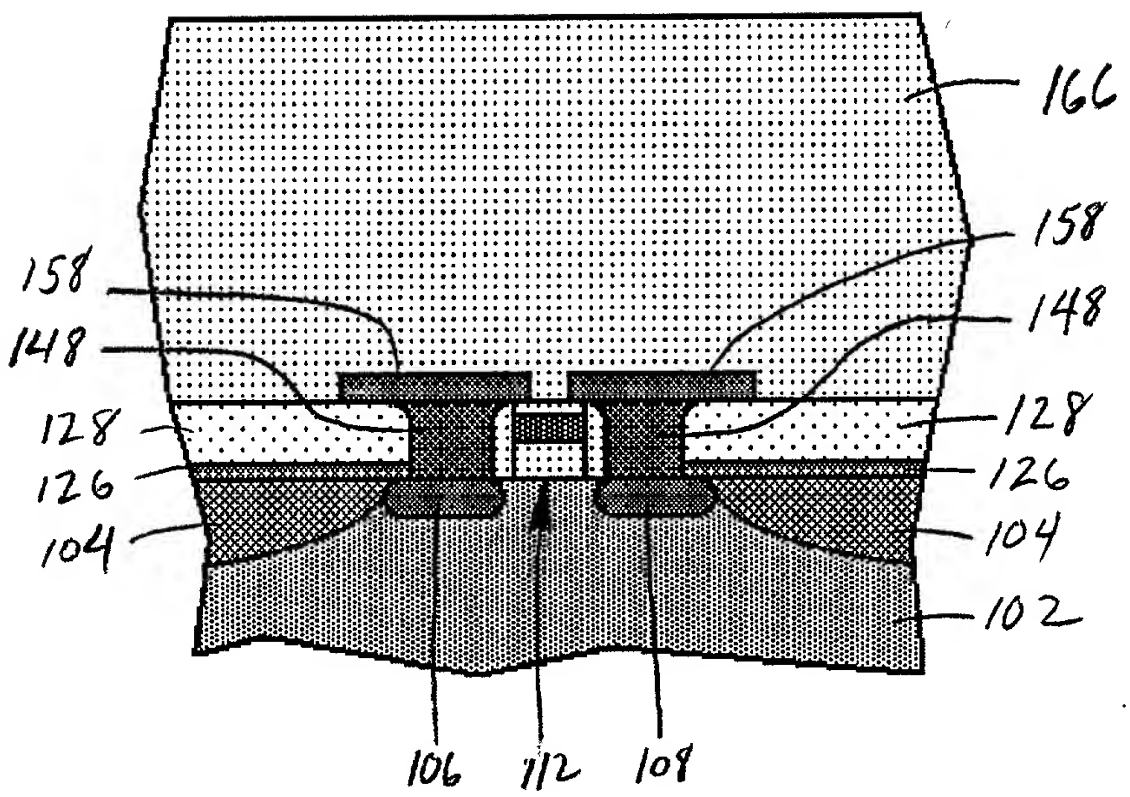

FIG. 18

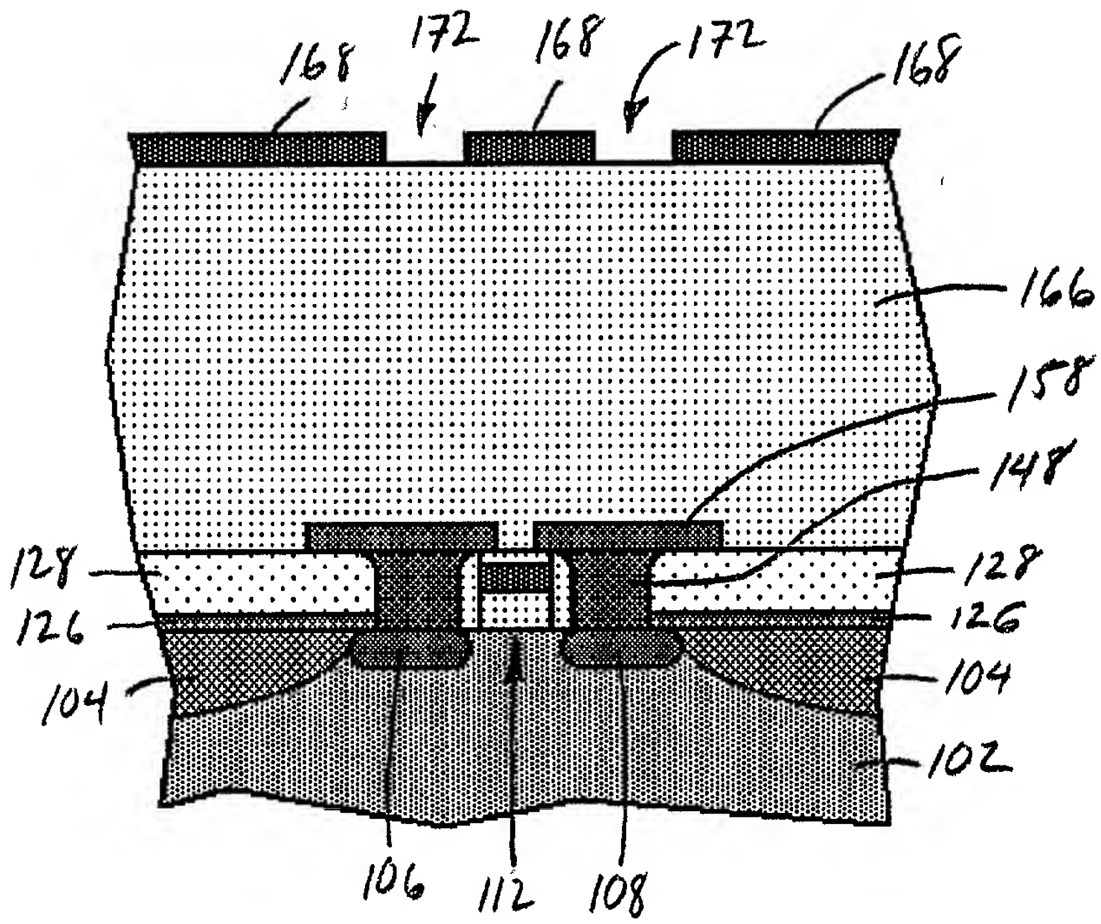

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FIG. 19

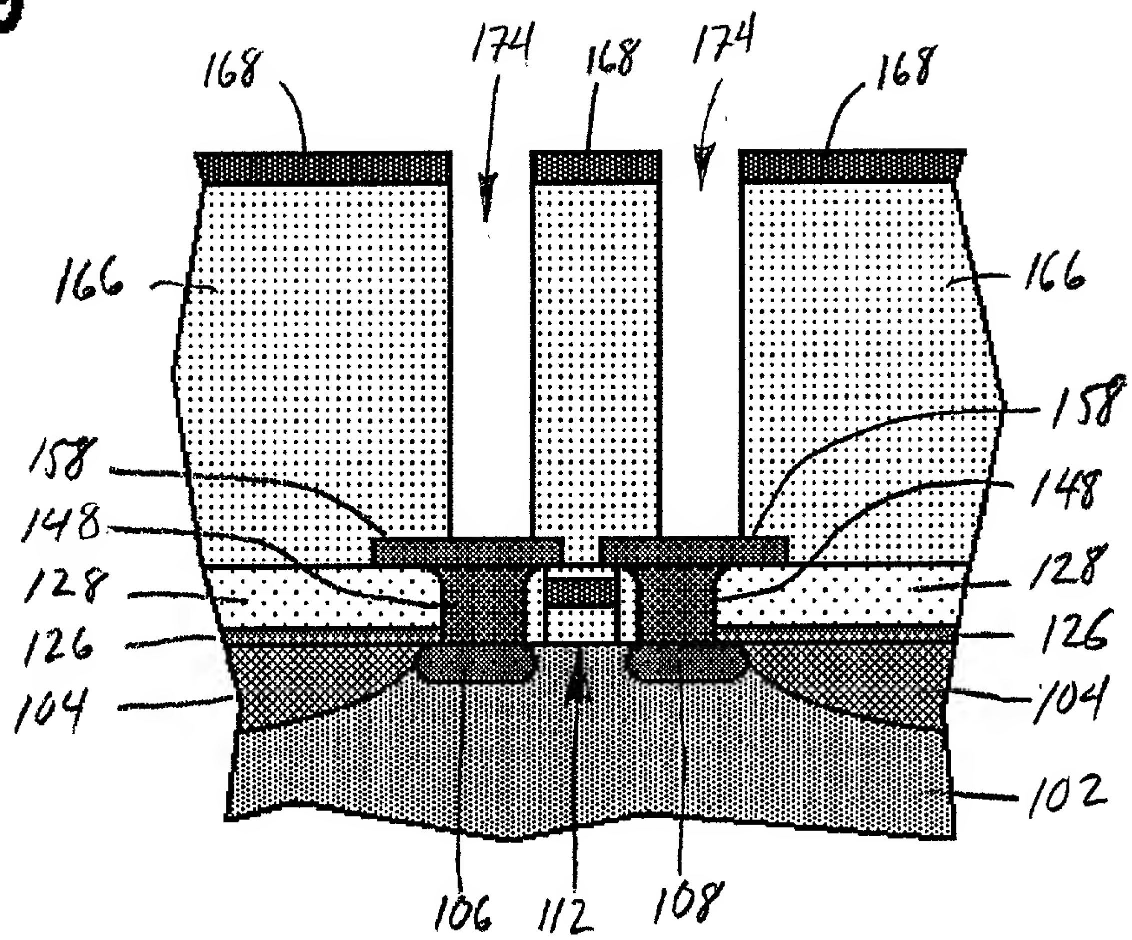
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FIG. 20

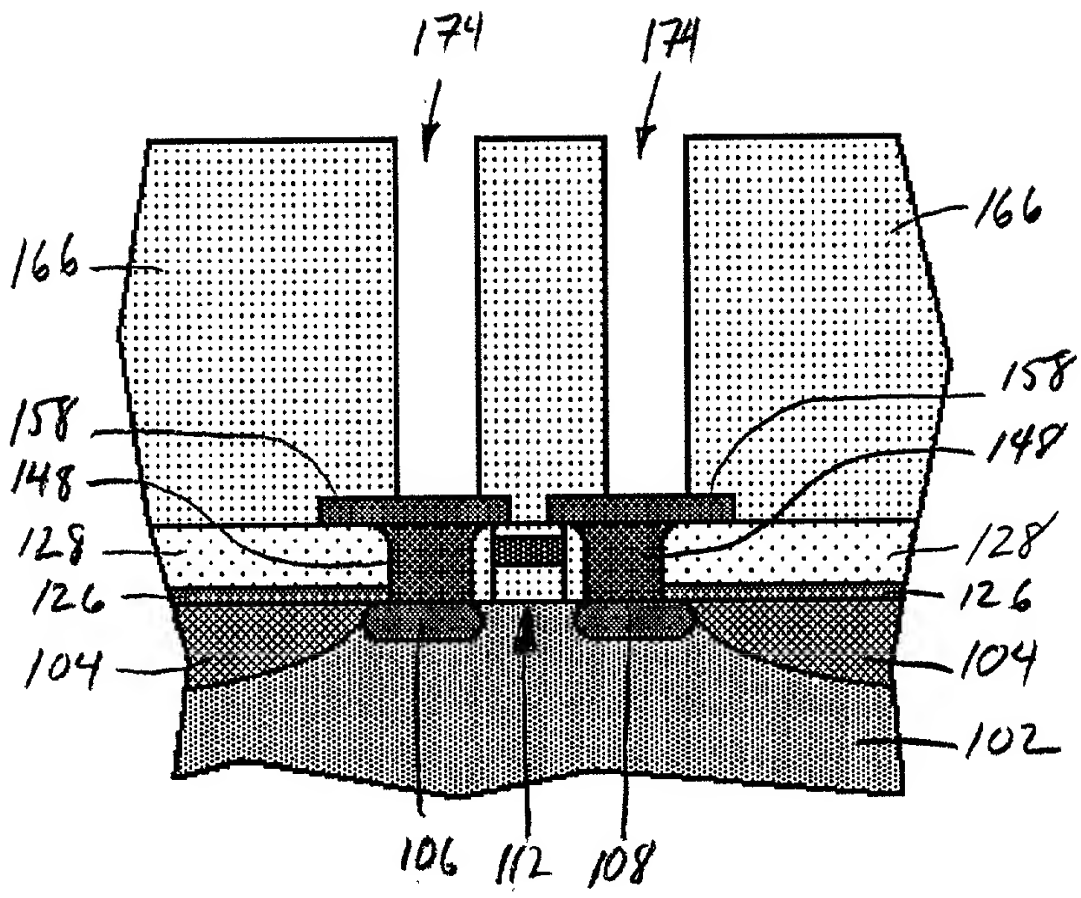

FIG. 21

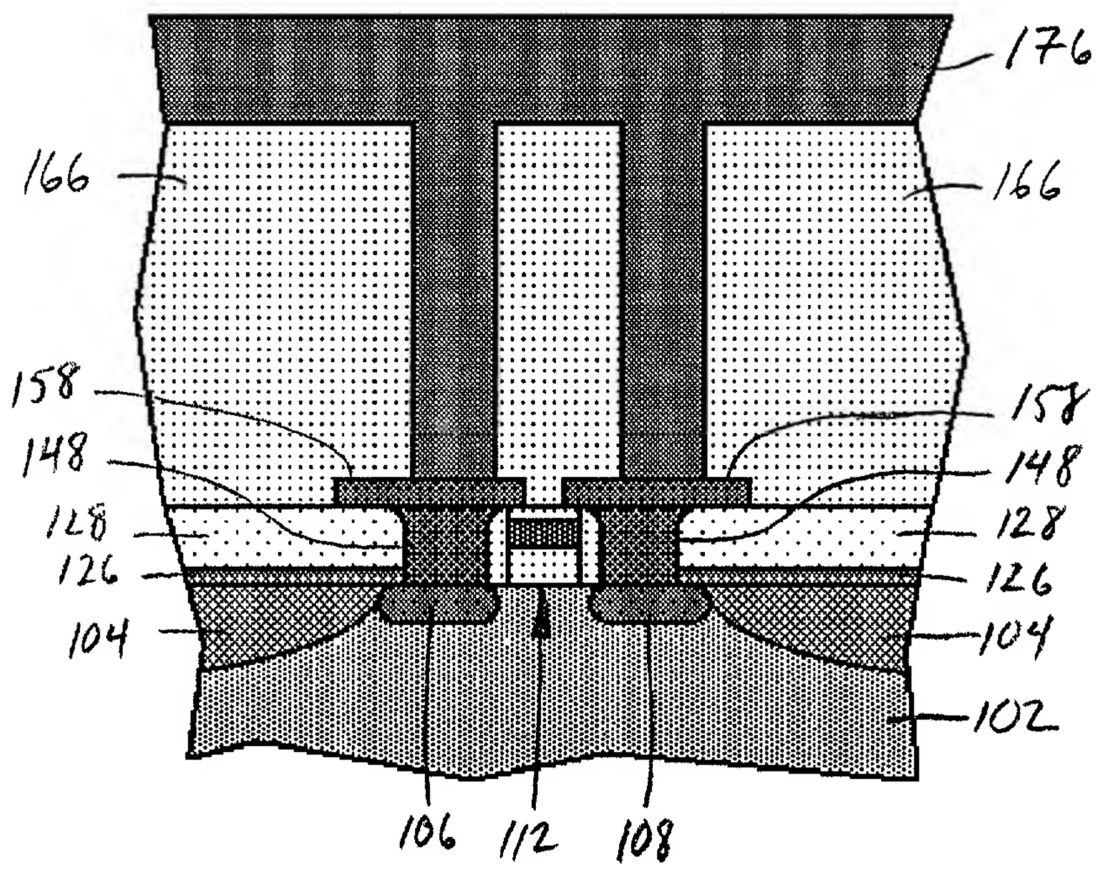

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FIG. 22

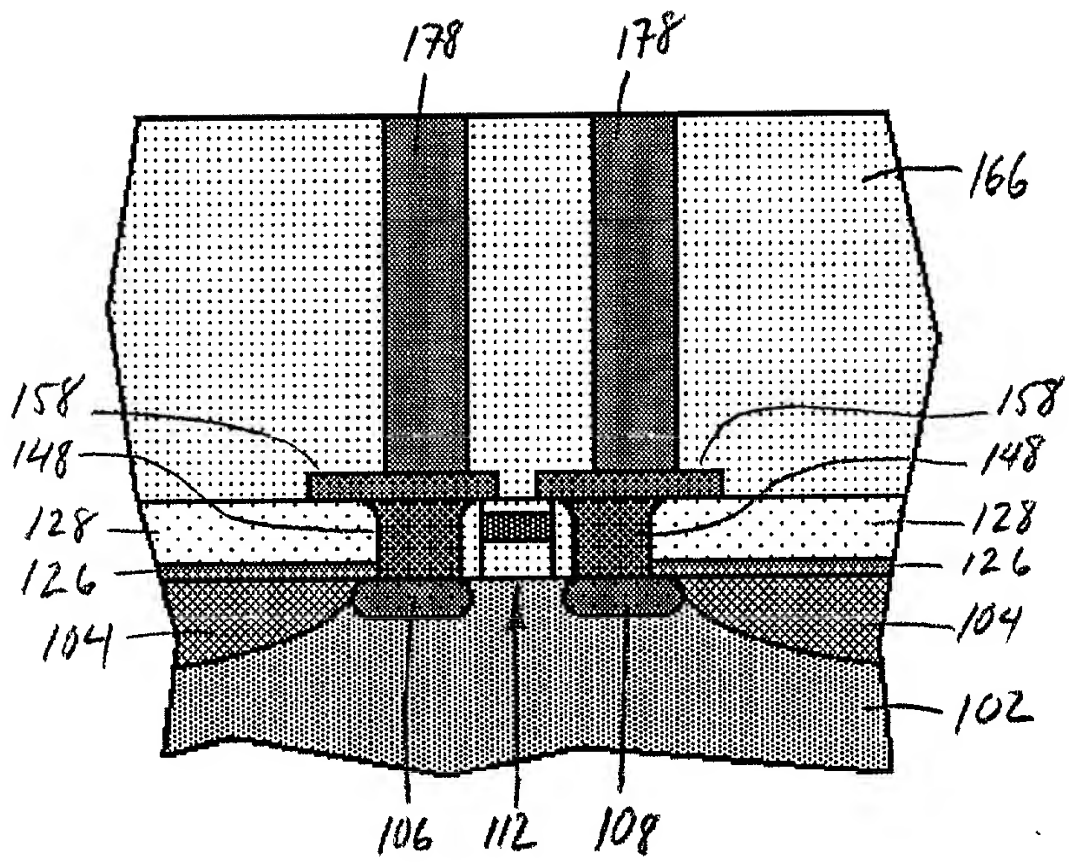
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FIG. 23

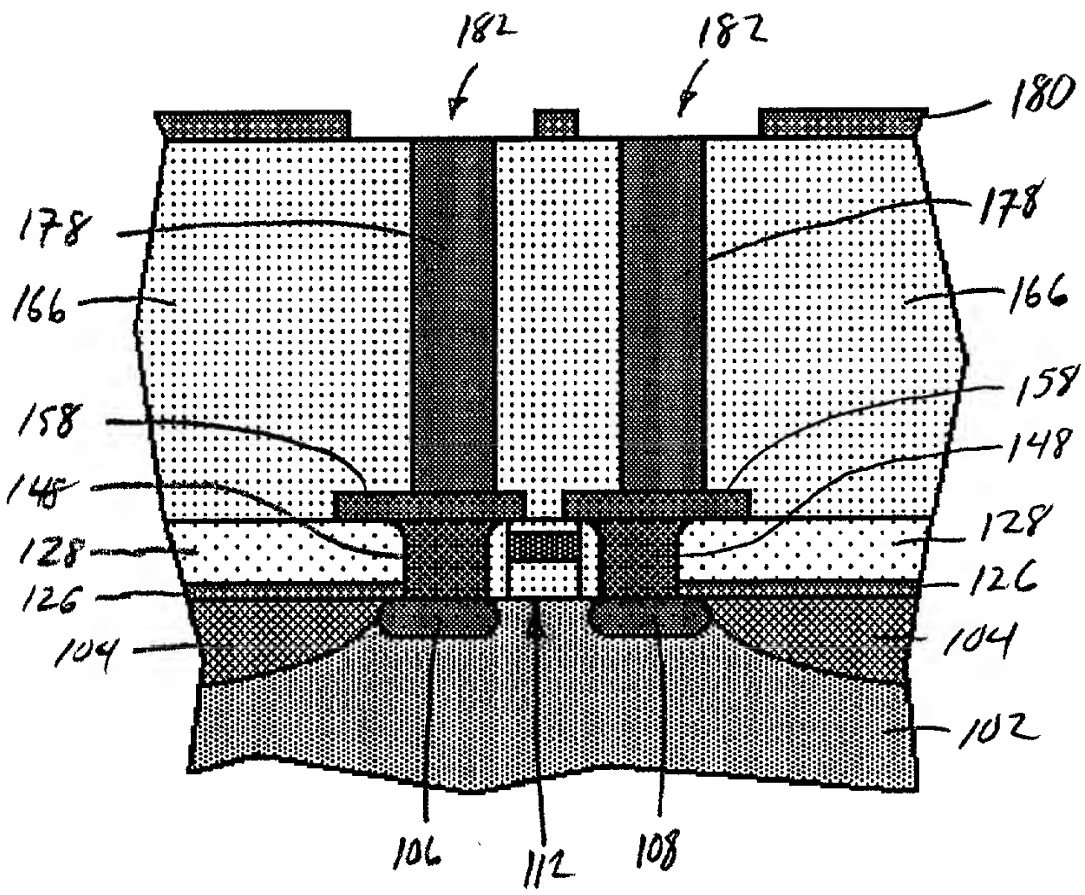
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FIG. 24

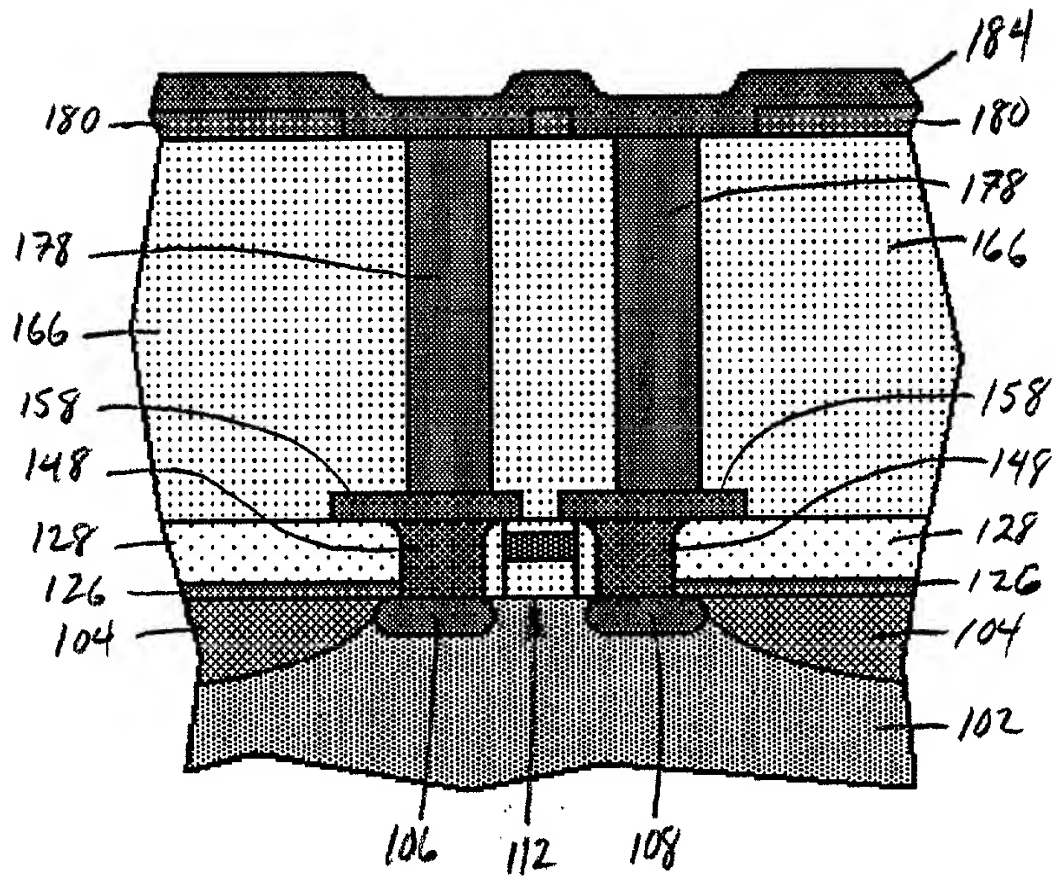
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FIG. 25

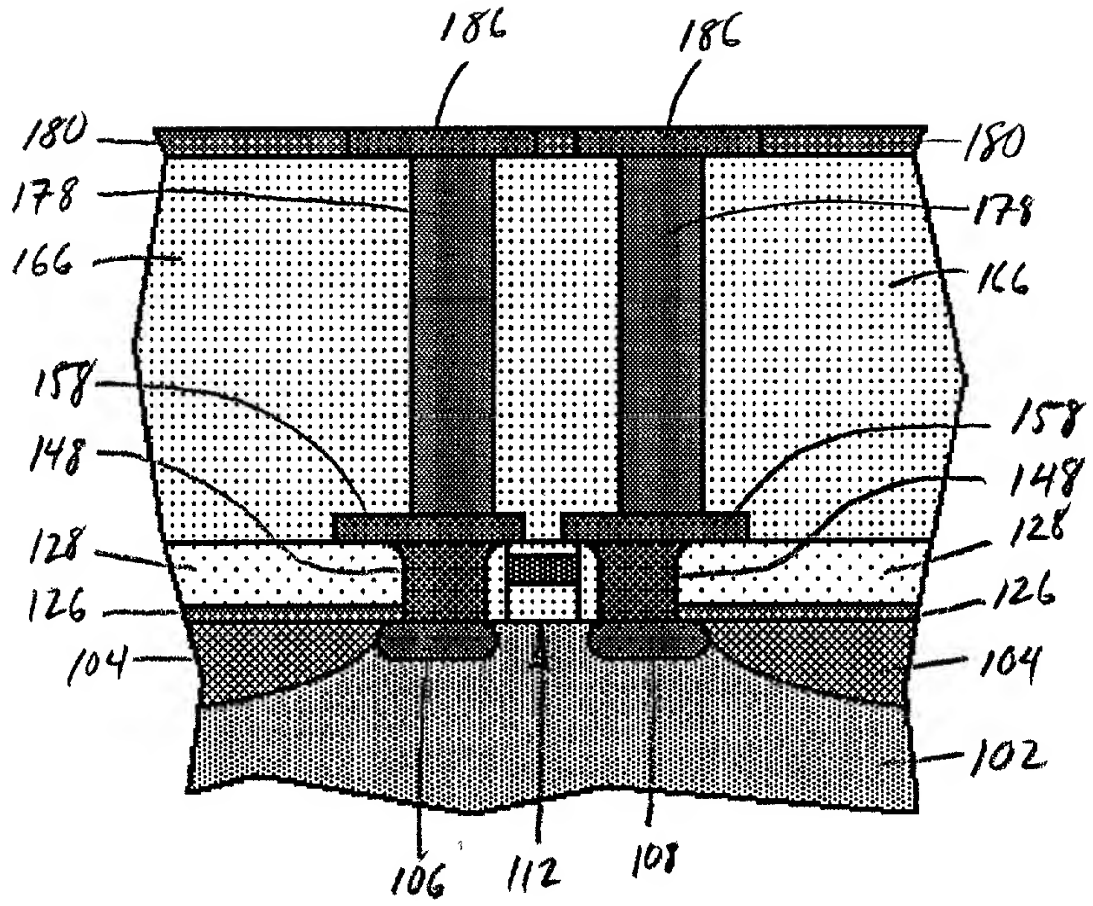
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FIG. 26

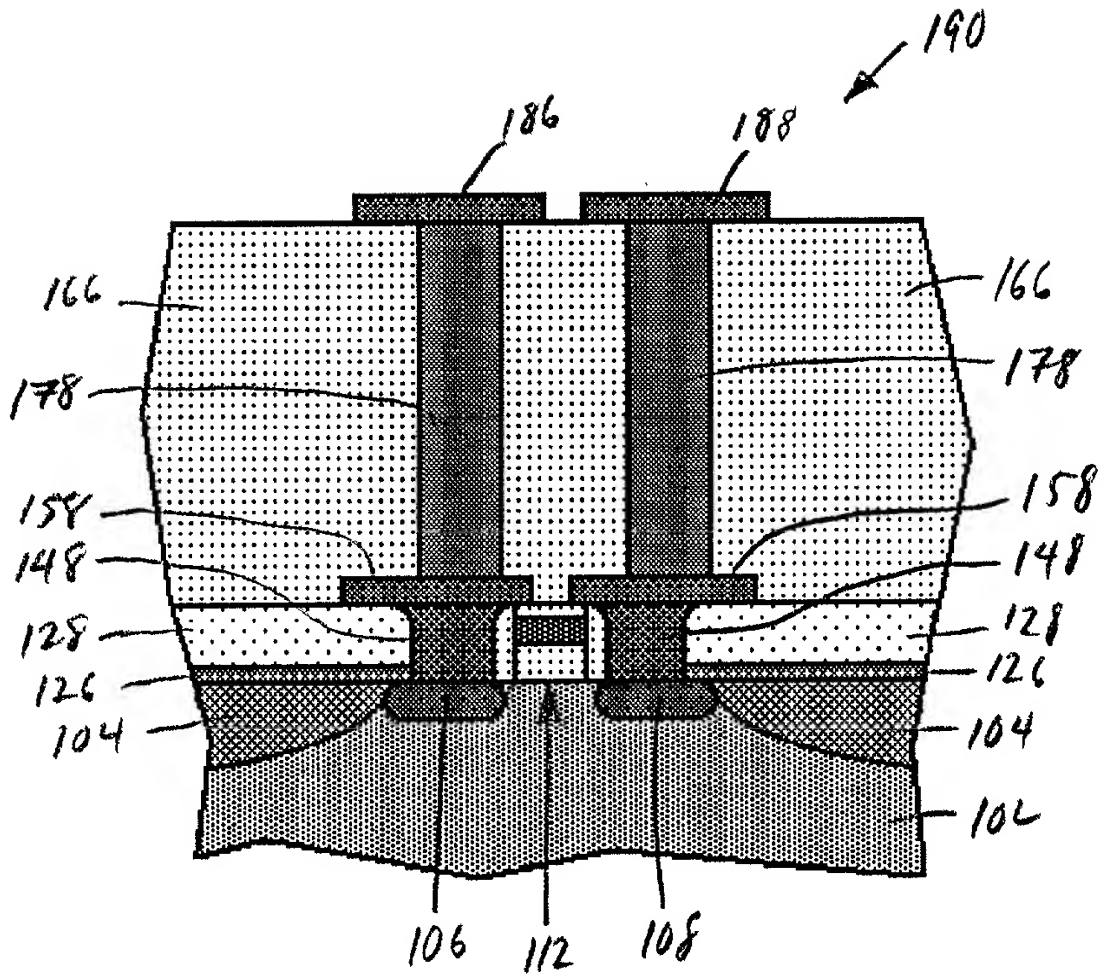
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FIG. 27

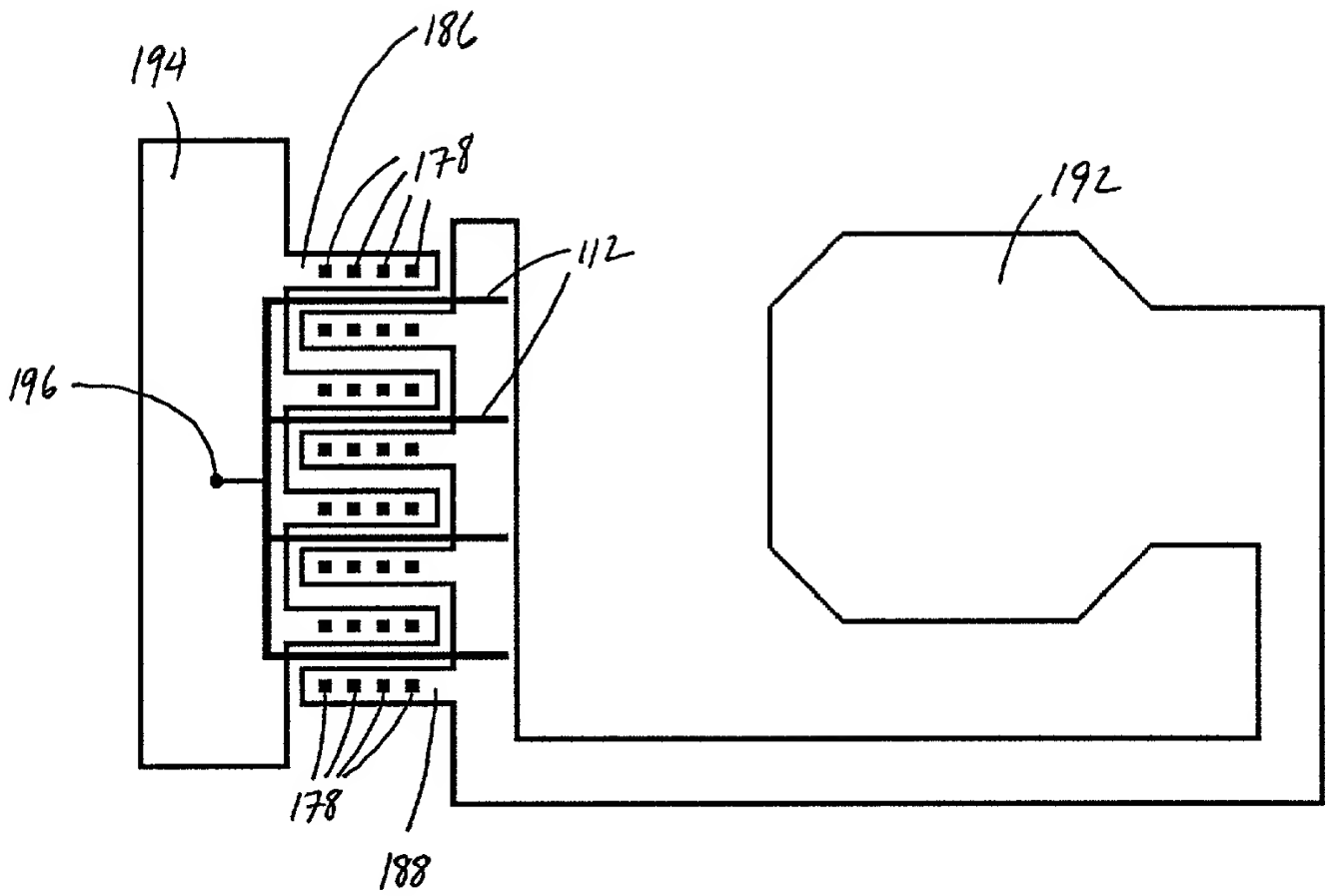

FIG. 28

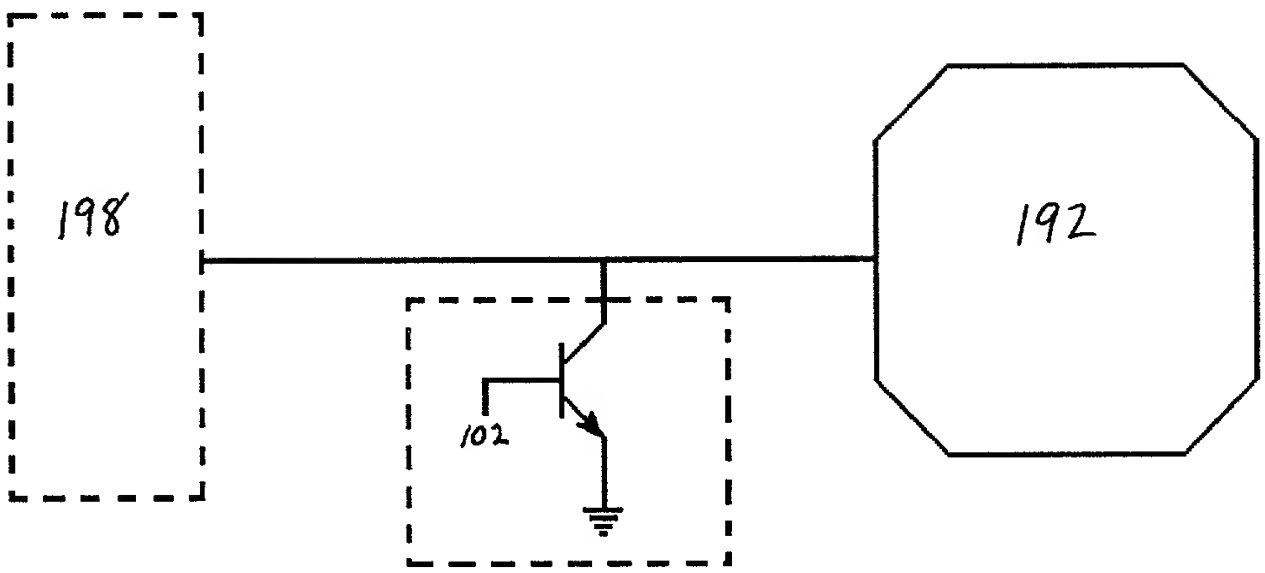

FIG. 29
PRIOR ART

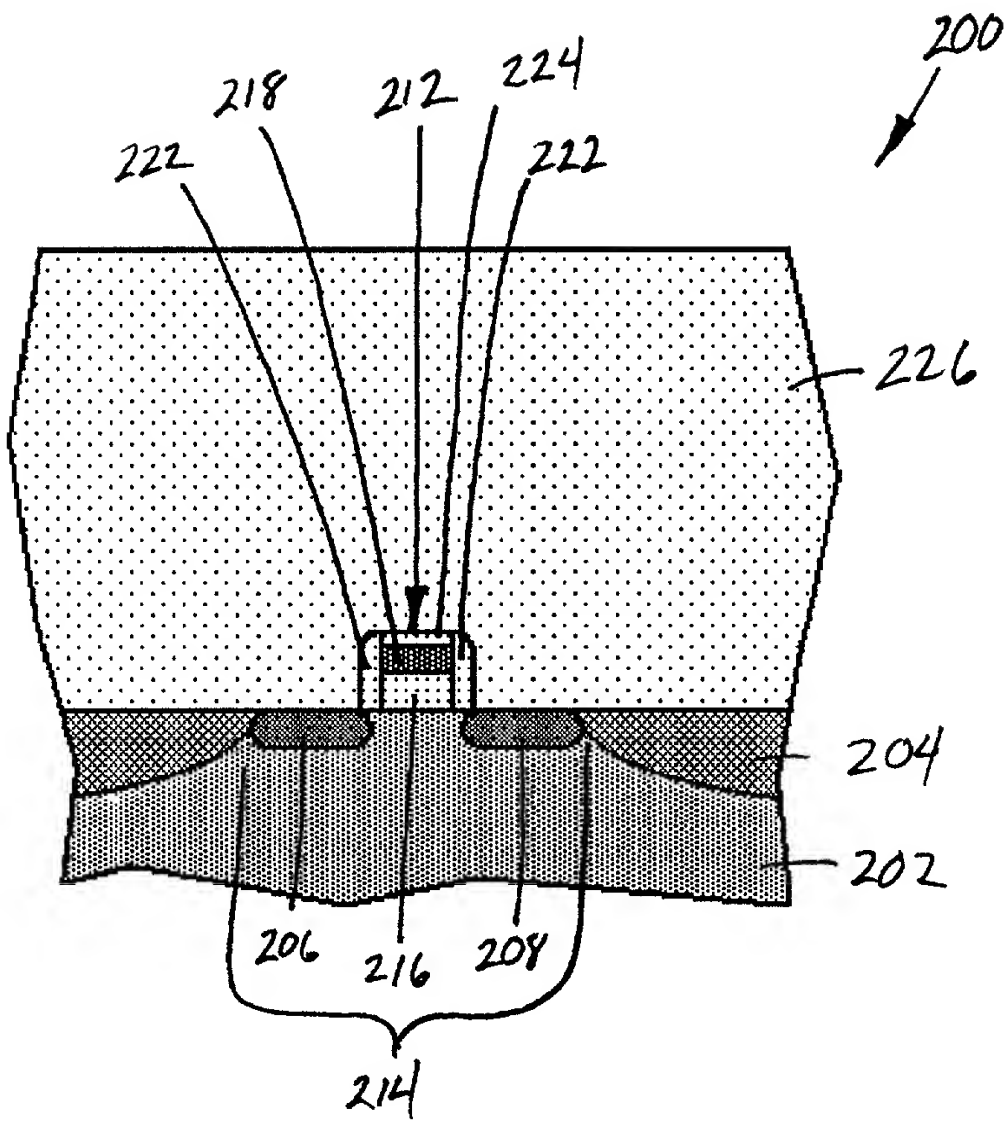

FIG. 30
PRIOR ART

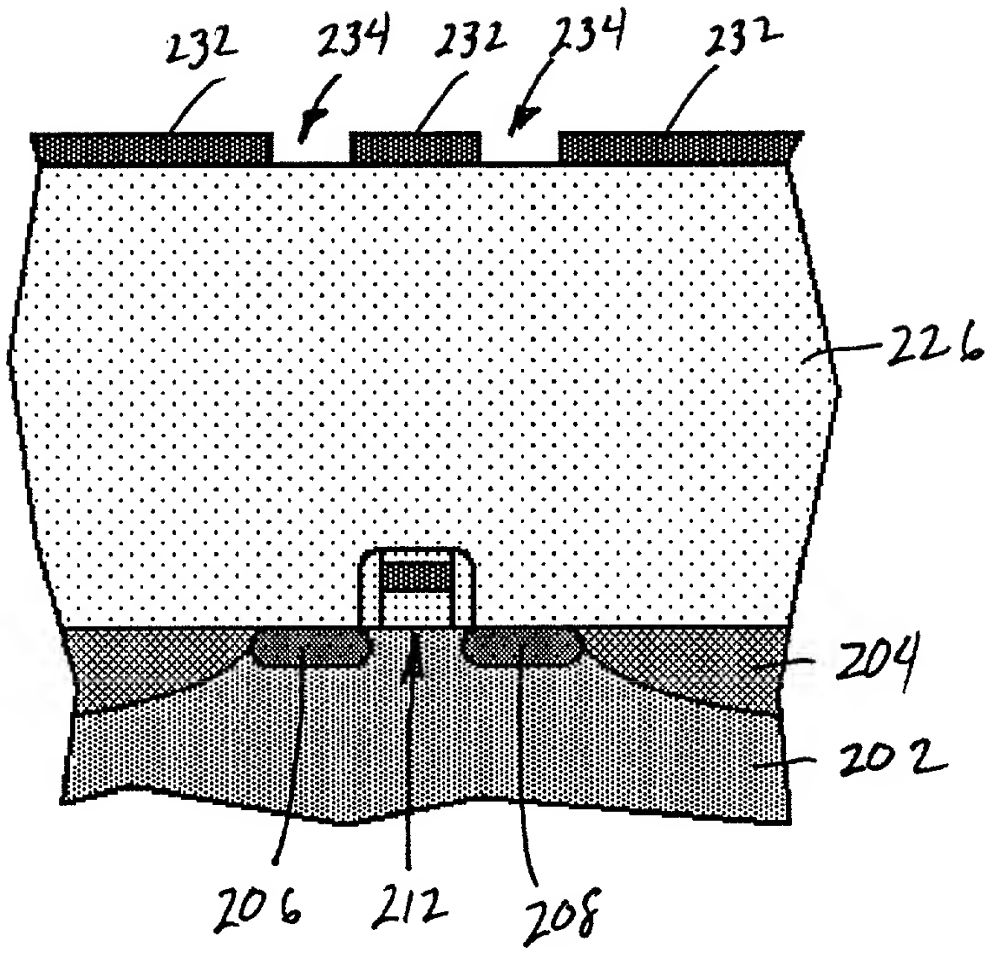

FIG. 31
PRIOR ART

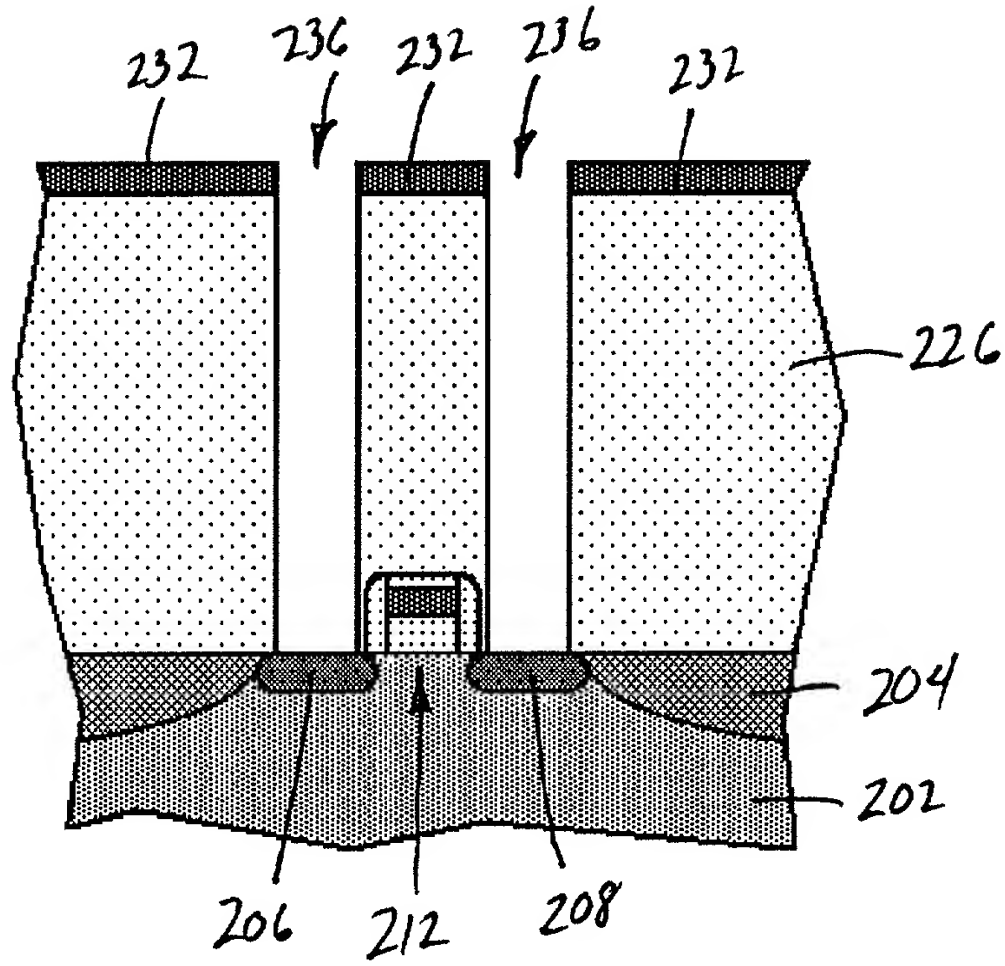

FIG. 32
PRIOR ART

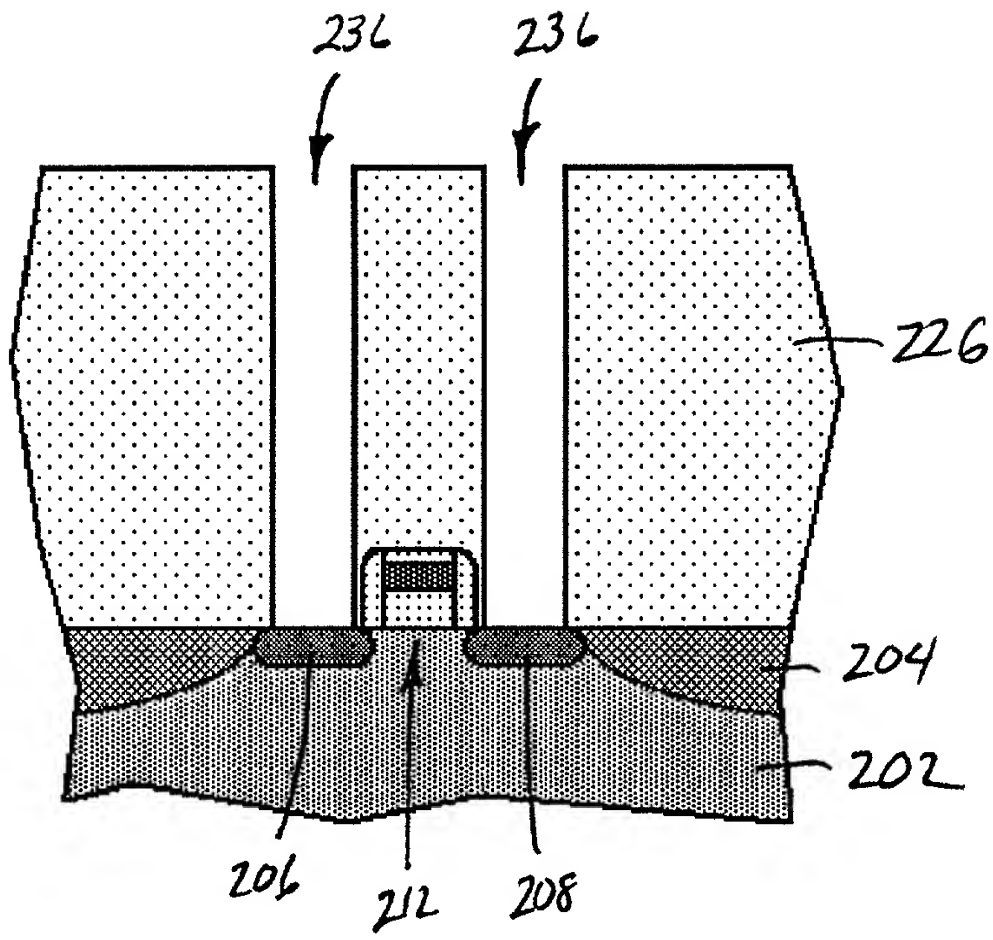

FIG. 33

PRIOR ART

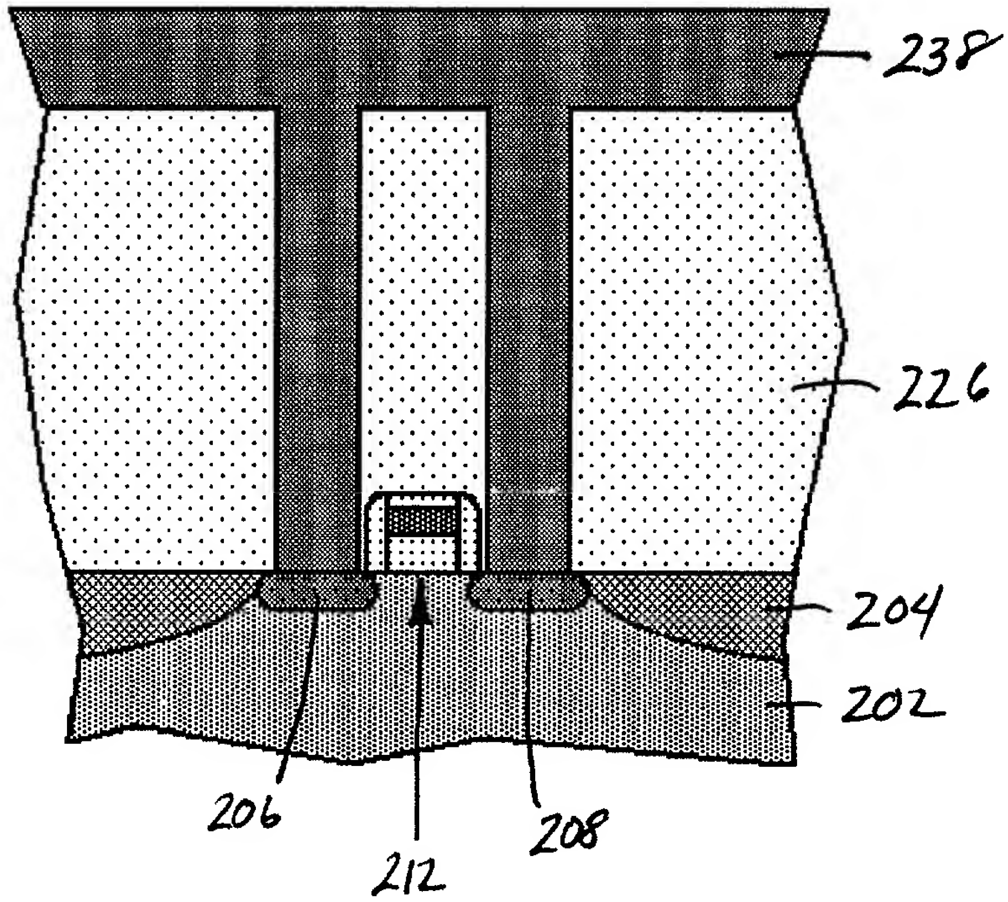

FIG. 34
PRIOR ART

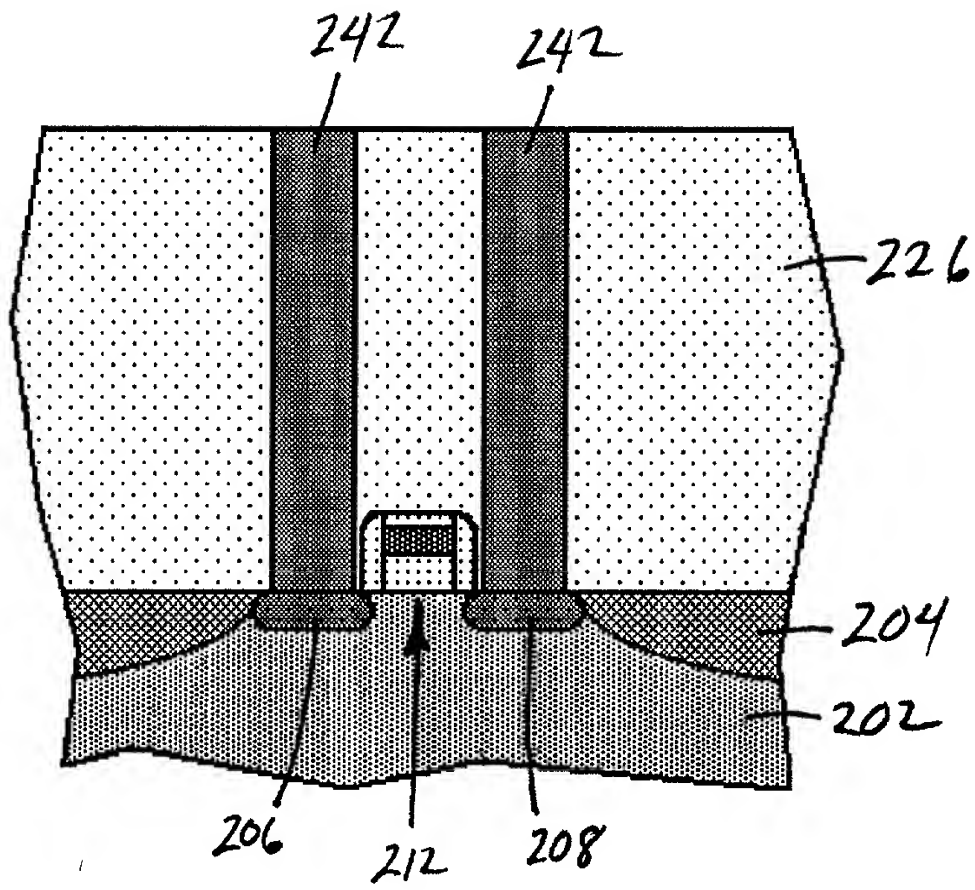

FIG. 35
PRIOR ART

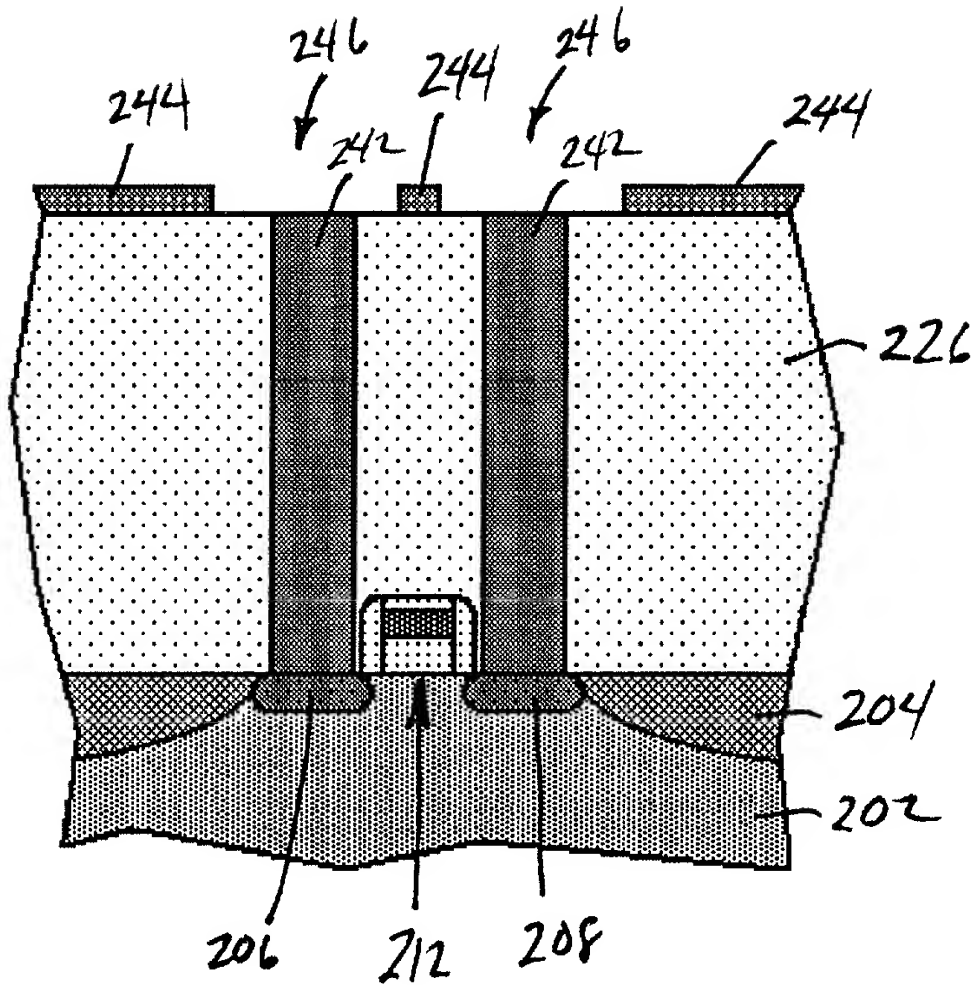

FIG. 36
PRIOR ART

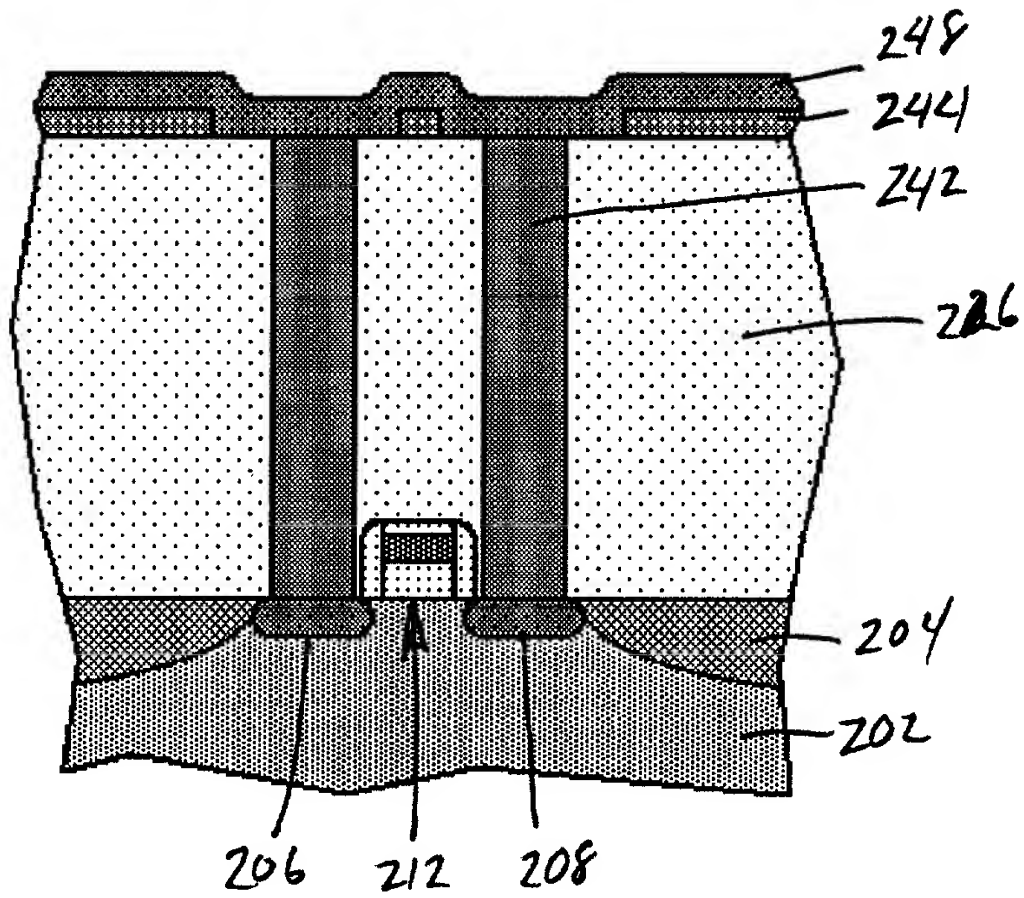

FIG. 37
PRIOR ART

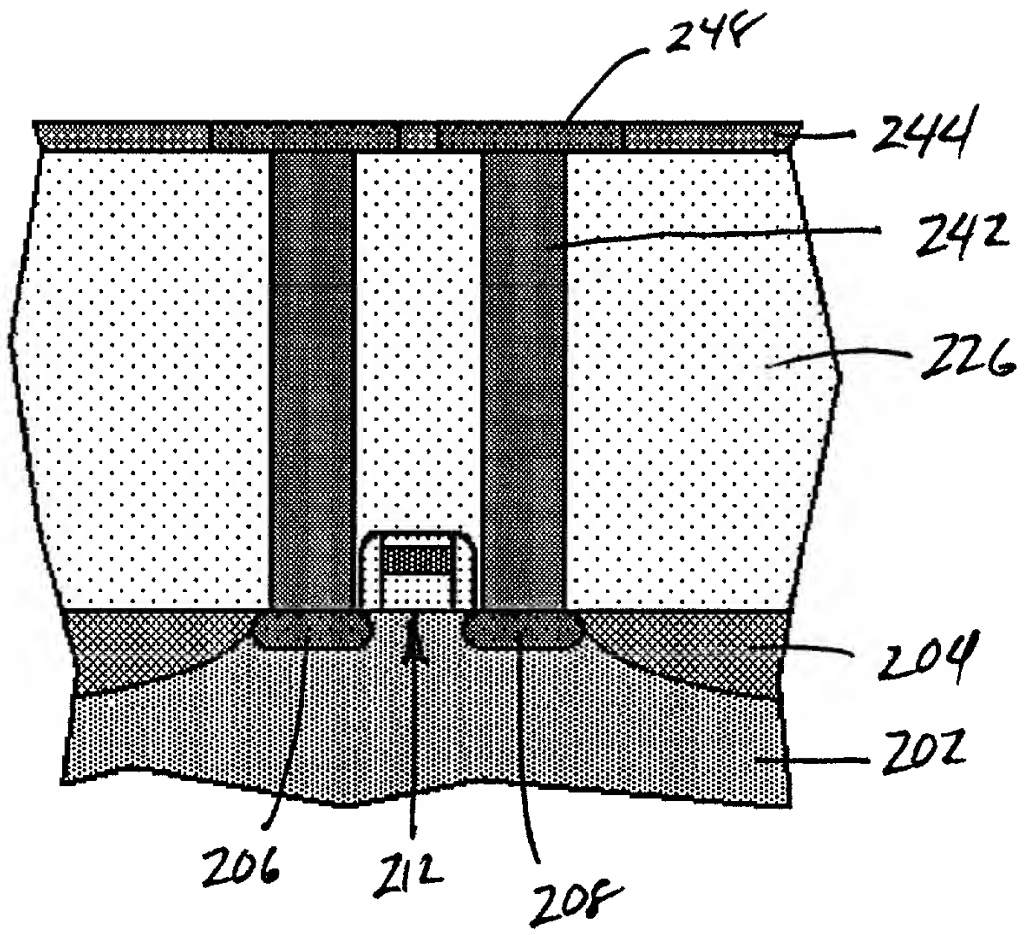

FIG. 38
PRIOR ART

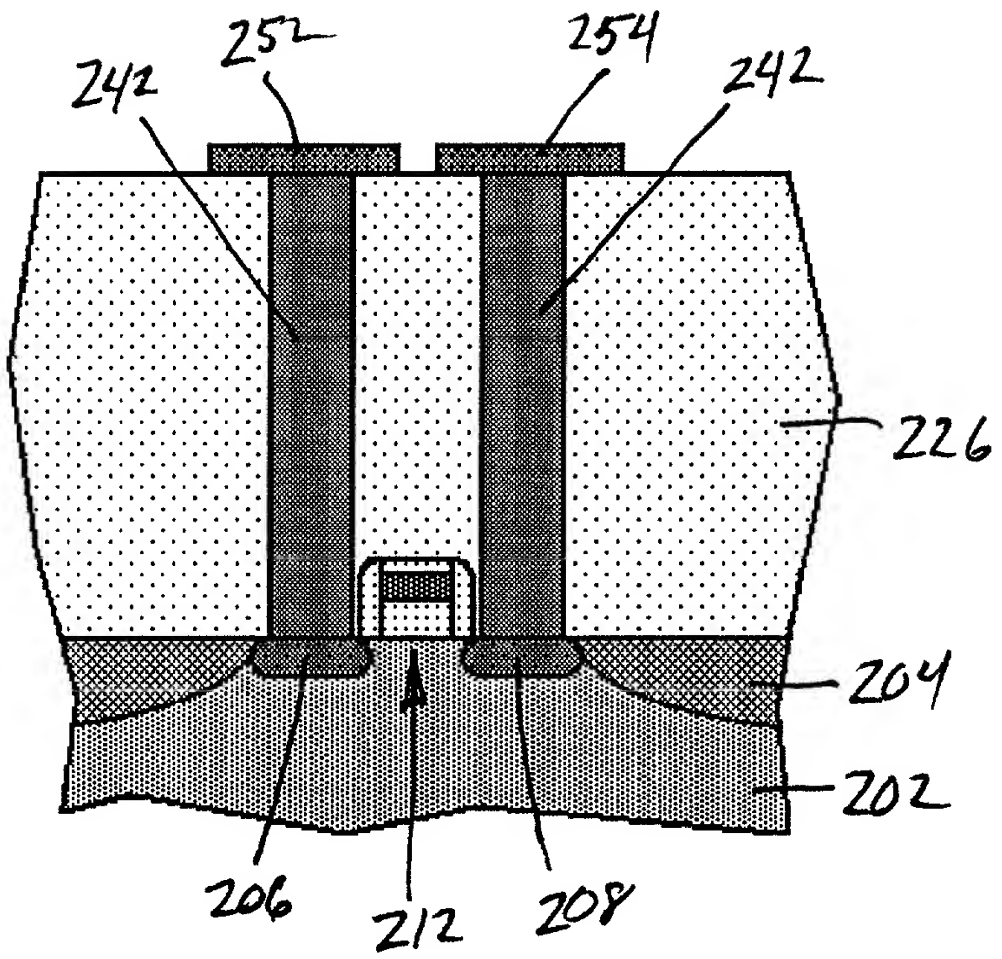

FIG. 39
PRIOR ART

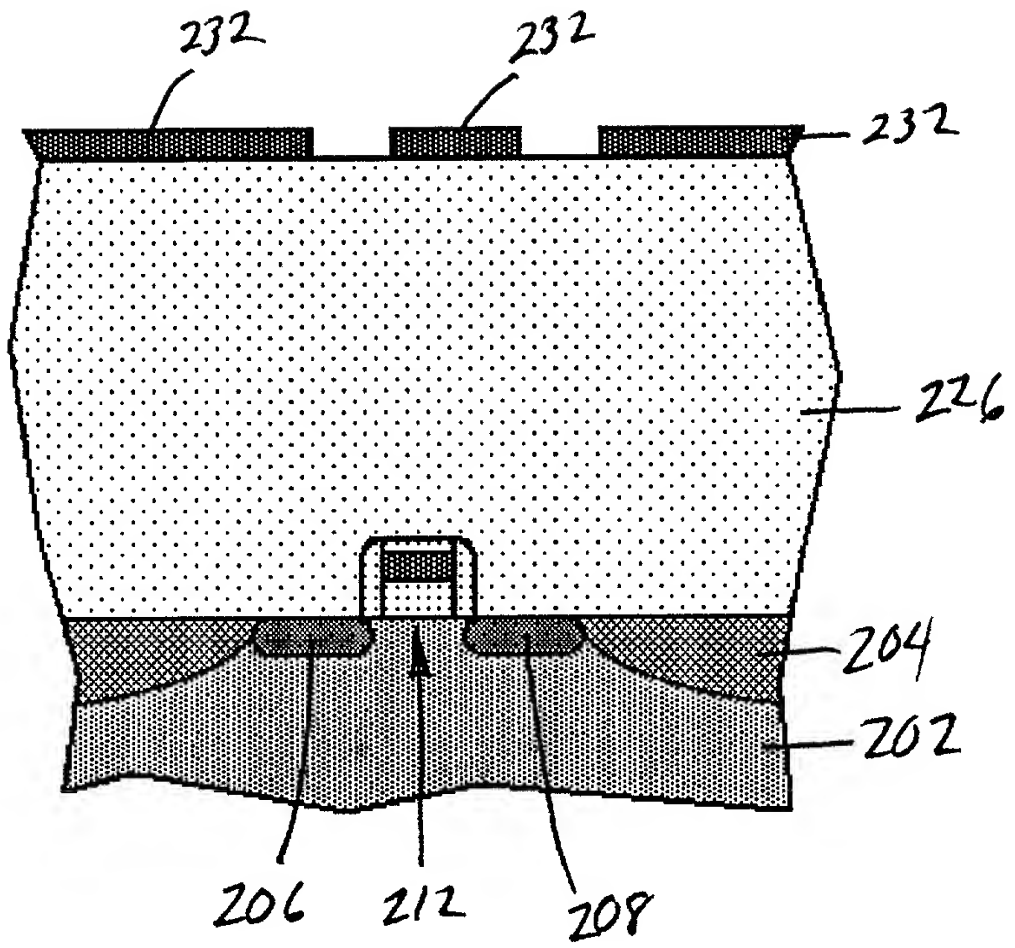

FIG. 40

PRIOR ART